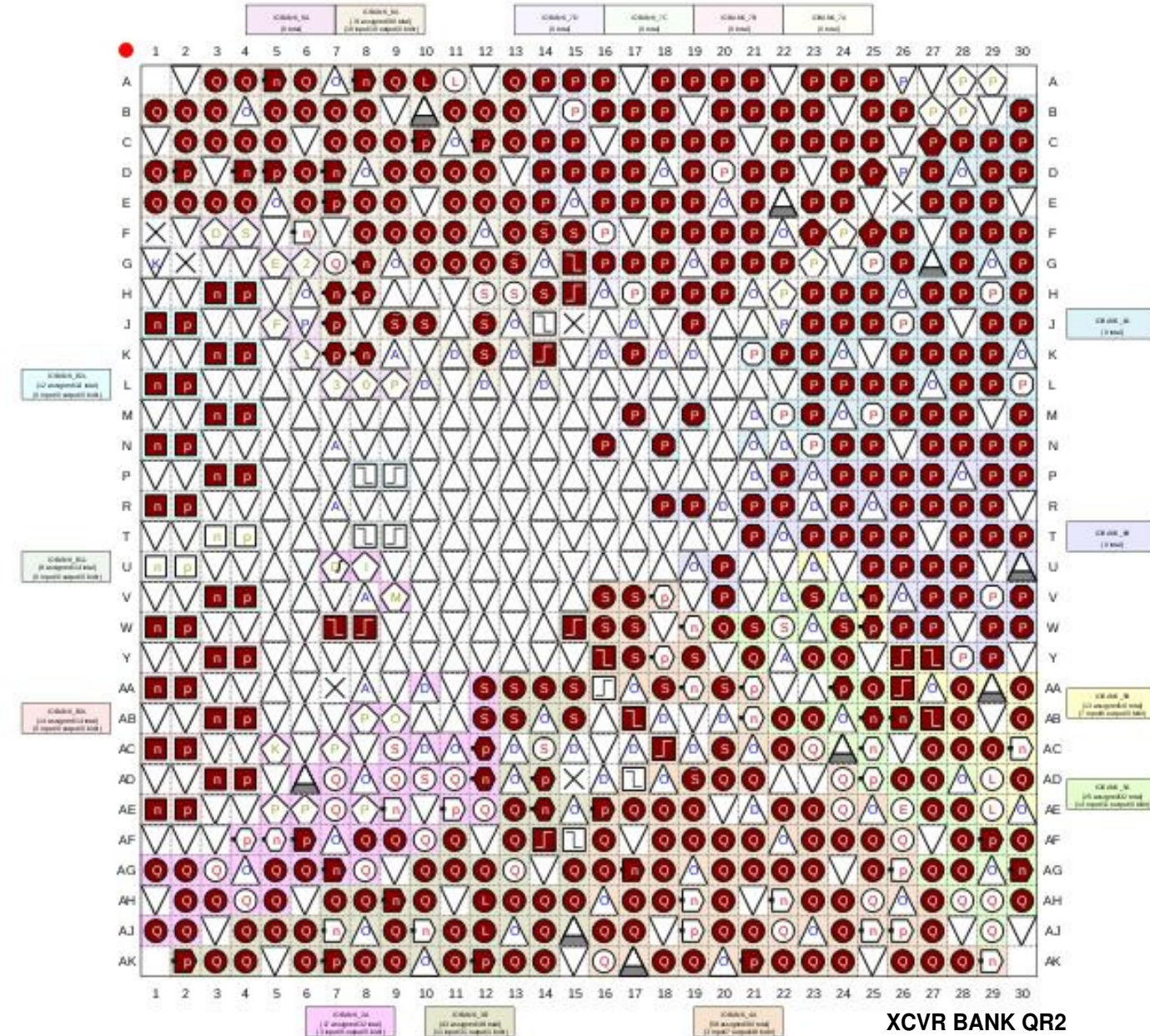


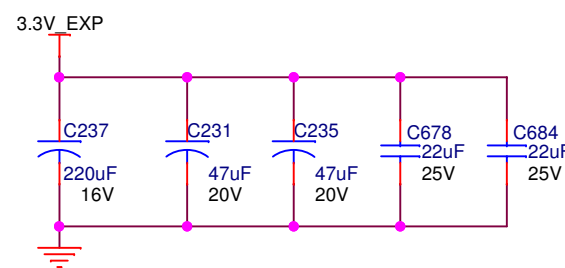
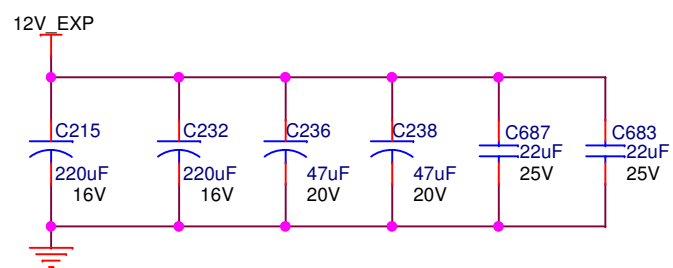
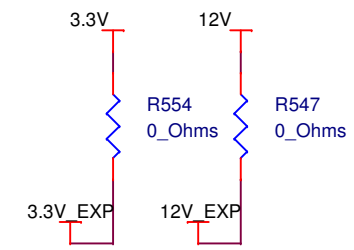
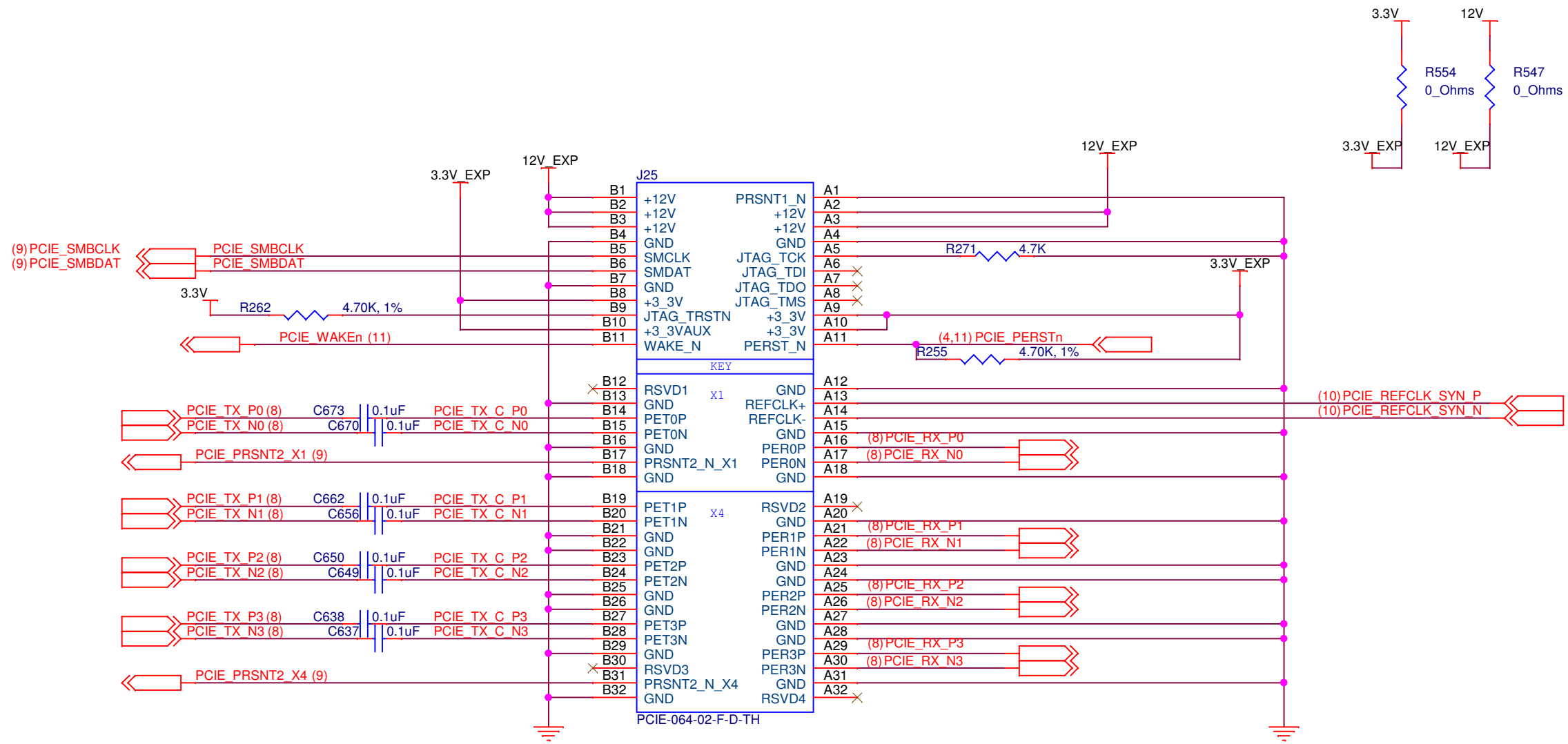
FPGA Package Top View

Top View - Wire Bond
Cyclone V - 5CSXFC6D6F31C7

I/O Bank Usage					
	I/O Bank	Usage	VCCIO Voltage	VREF Voltage	VCCPD Voltage
1	B2L	0 / 14 (0 %)	--	--	--
2	B1L	0 / 14 (0 %)	--	--	--
3	B0L	0 / 14 (0 %)	--	--	--
4	3A	28 / 32 (88 %)	2.5V	--	2.5V
5	3B	43 / 48 (90 %)	1.5V	0.75V	2.5V
6	4A	58 / 80 (73 %)	1.5V	0.75V	2.5V
7	5A	25 / 32 (78 %)	2.5V	--	2.5V
8	5B	13 / 16 (81 %)	2.5V	--	2.5V
9	6B	34 / 45 (76 %)	1.5V	0.75V	2.5V
10	6A	48 / 57 (84 %)	1.5V	0.75V	2.5V
11	7A	19 / 19 (100 %)	3.3V	--	3.3V
12	7B	20 / 22 (91 %)	3.3V	--	3.3V
13	7C	12 / 12 (100 %)	3.3V	--	3.3V
14	7D	12 / 14 (86 %)	3.3V	--	3.3V
15	8A	74 / 80 (93 %)	2.5V	--	2.5V

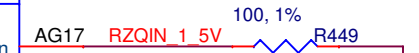
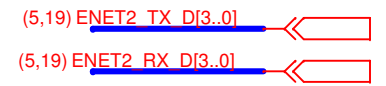
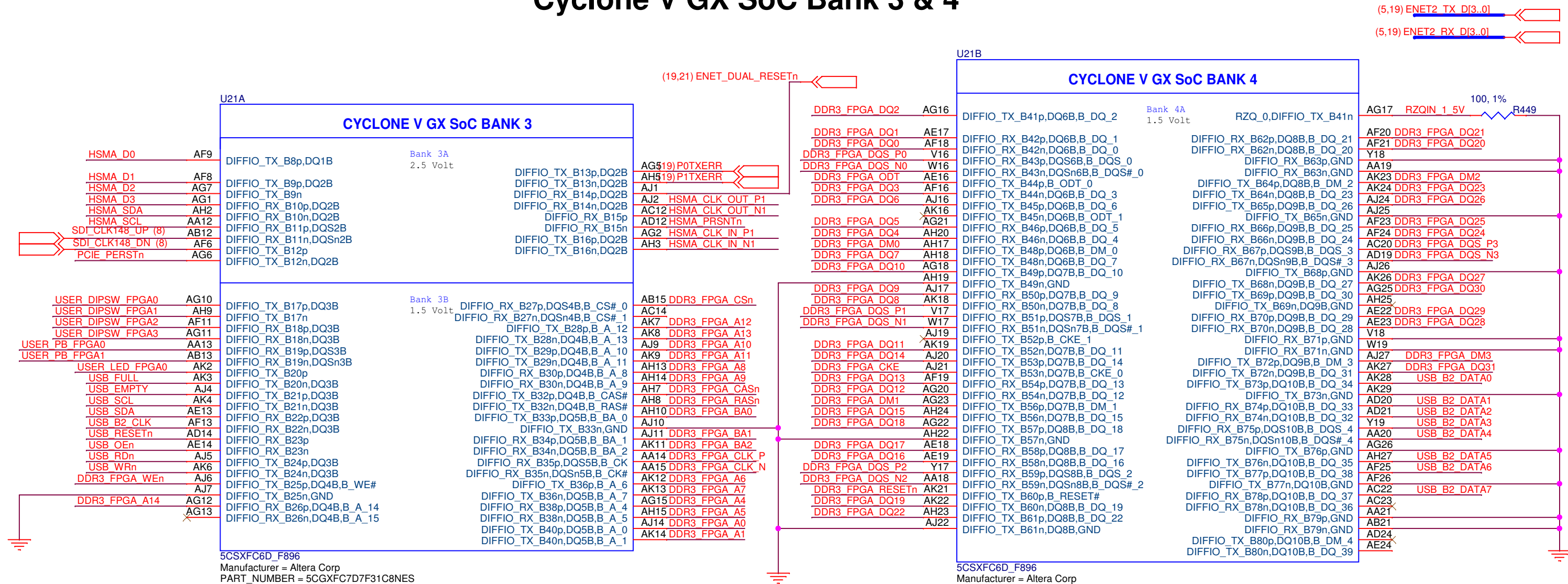


PCI Express Connector

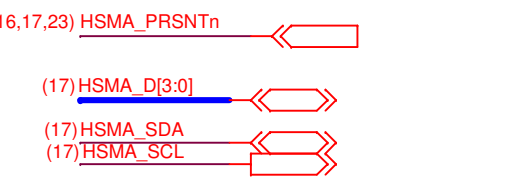
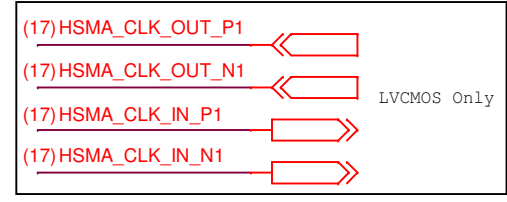


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Size: B	Document Number: 150-0321003-D1	Rev: D1
Date: Wednesday, November 20, 2013	Sheet: 3	of 41

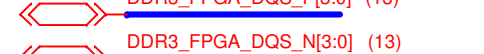
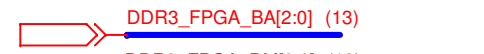
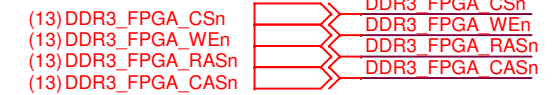
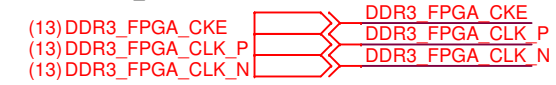
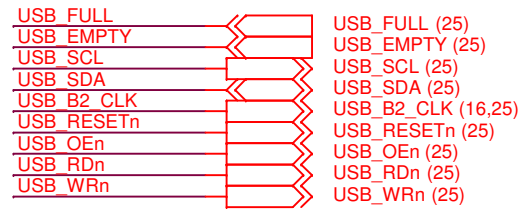
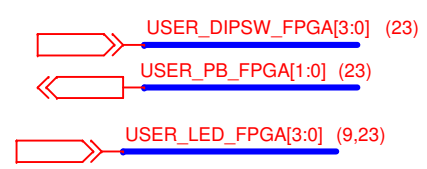
Cyclone V GX SoC Bank 3 & 4



HSMC LVCMOS INTERFACE

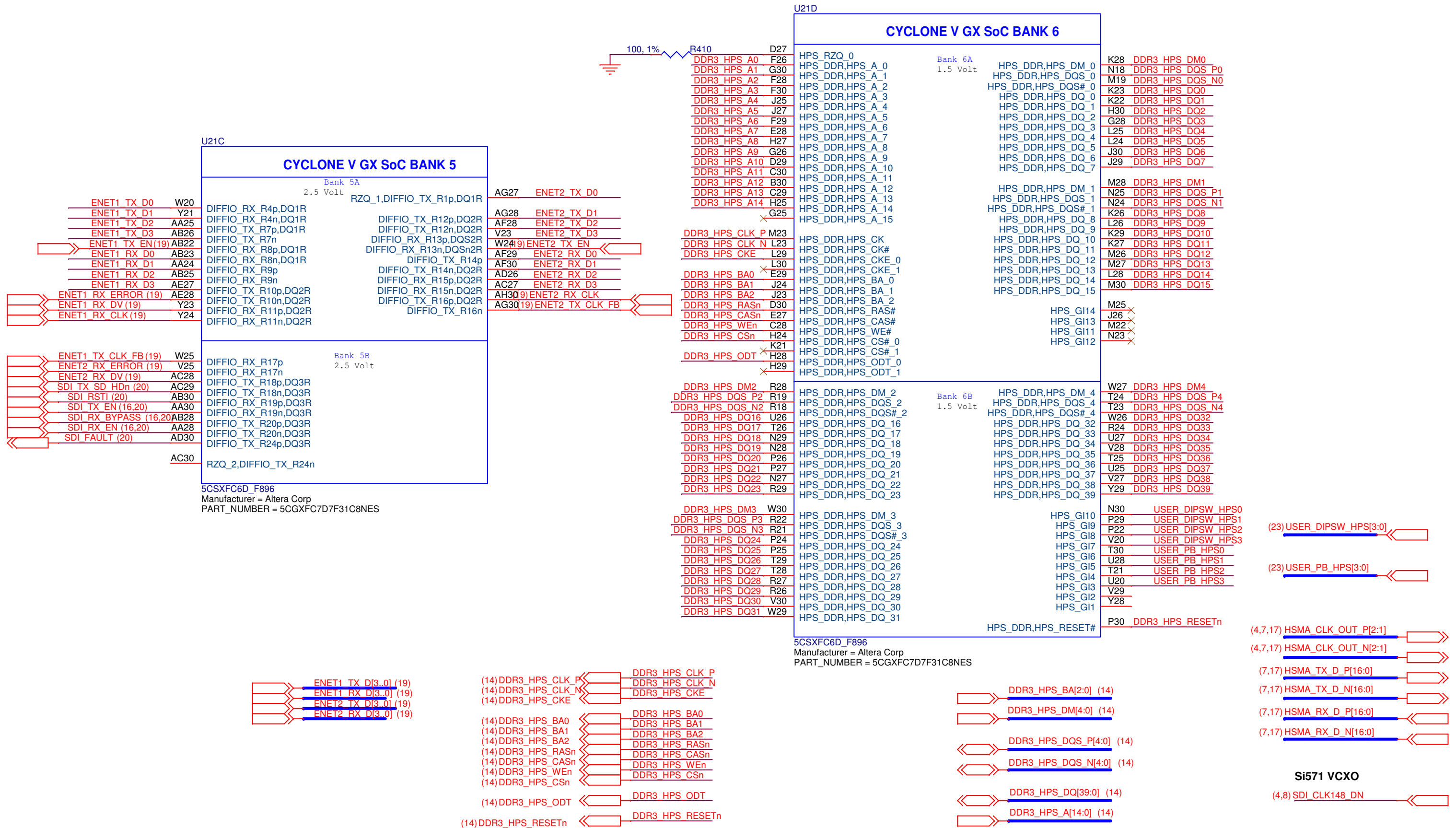


PCIE INTERFACE



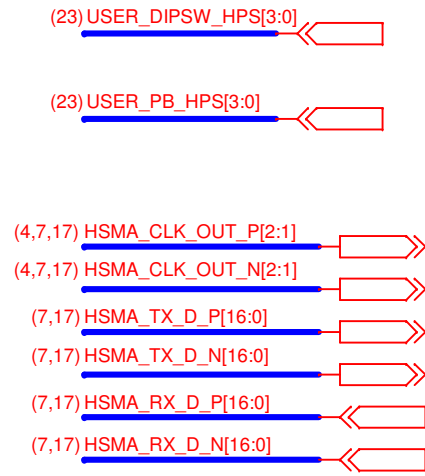
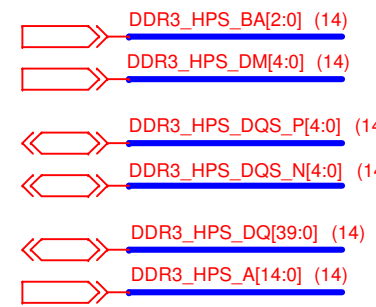
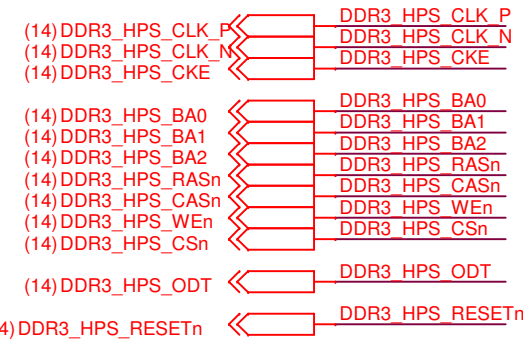
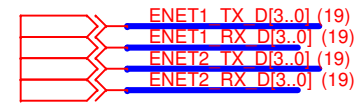
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Cyclone V GX SoC Bank 5 & 6



5CSXFC6D_F896
 Manufacturer = Altera Corp
 PART_NUMBER = 5CGXFC7D7F31C8NES

5CSXFC6D_F896
 Manufacturer = Altera Corp
 PART_NUMBER = 5CGXFC7D7F31C8NES



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Cyclone V GX SoC Bank 7

Micro SD / USB INTERFACE

USB_DATA[7..0] ↔ USB_DATA[7..0] (22)

ETHERNET INTERFACE

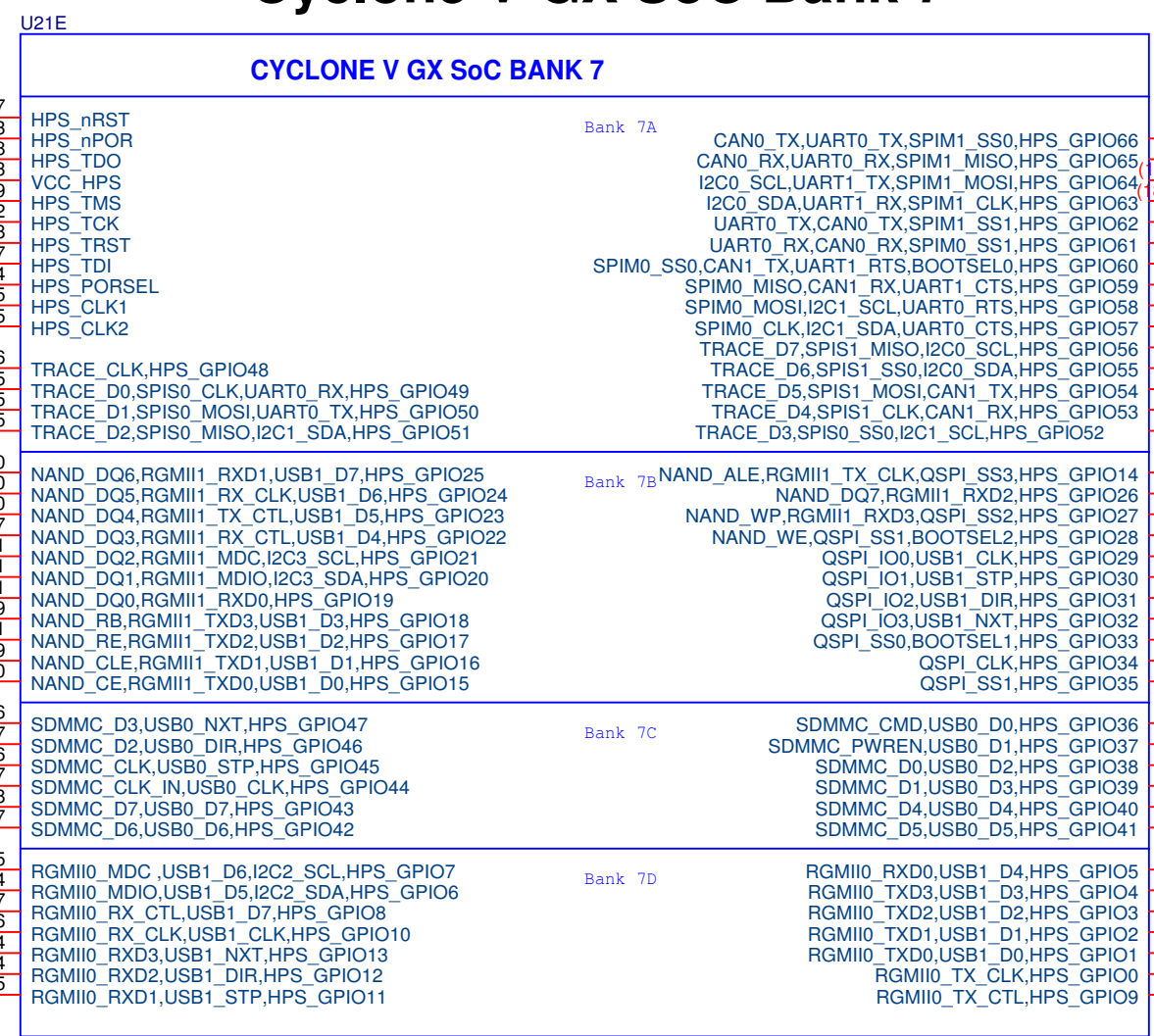
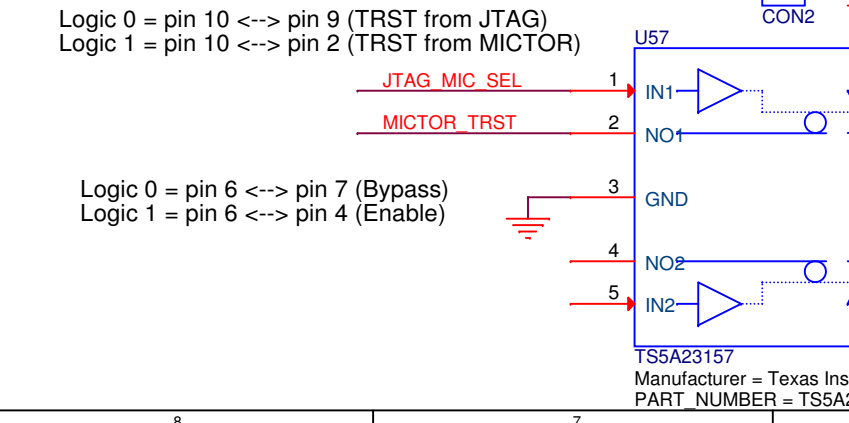
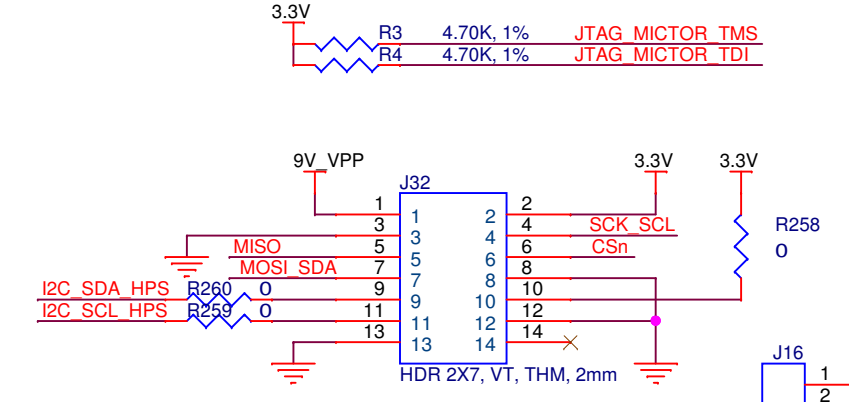
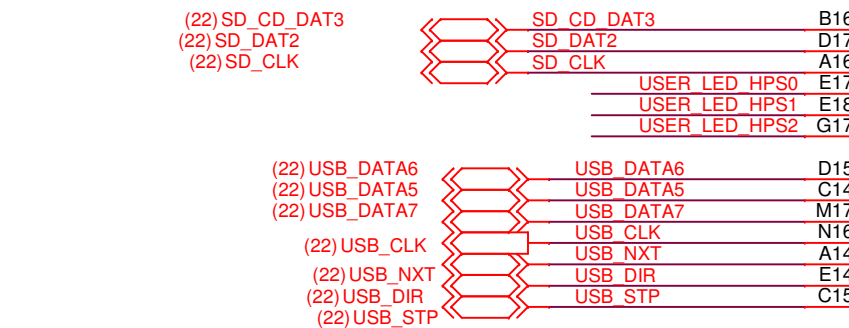
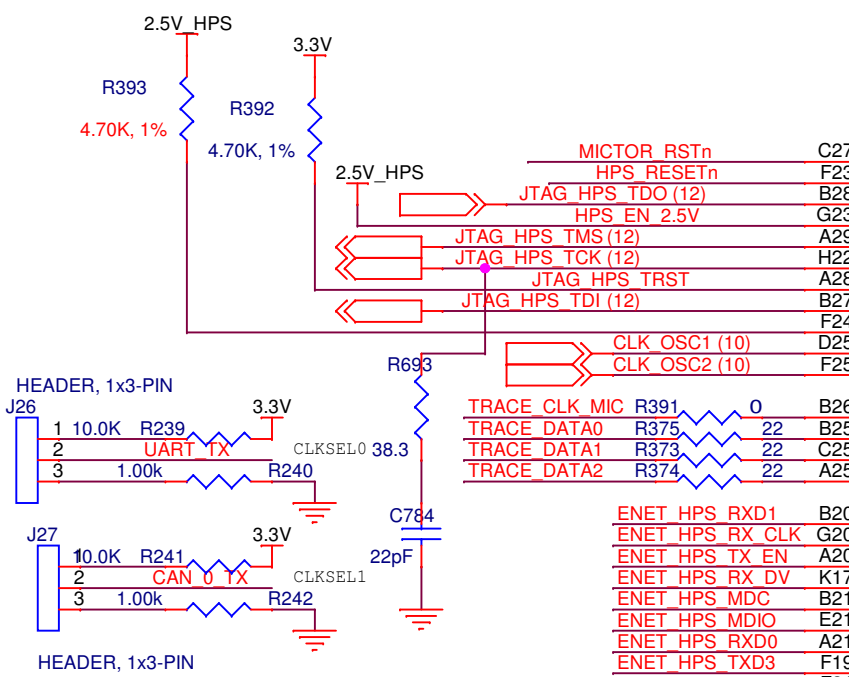
ENET_HPS_TXD[3..0] ↔ ENET_HPS_TXD[3..0] (18)
 ENET_HPS_GTX_CLK ↔ ENET_HPS_GTX_CLK (18)
 ENET_HPS_TX_EN ↔ ENET_HPS_TX_EN (18)
 ENET_HPS_MDC ↔ ENET_HPS_MDC (18)
 ENET_HPS_RESETn ↔ ENET_HPS_RESETn (18,21)

ENET_HPS_RXD[3..0] ↔ ENET_HPS_RXD[3..0] (18)

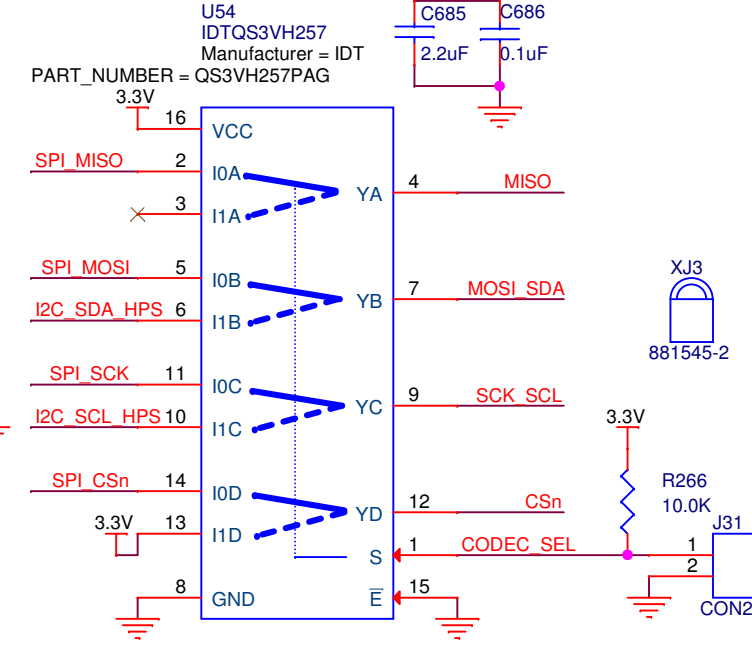
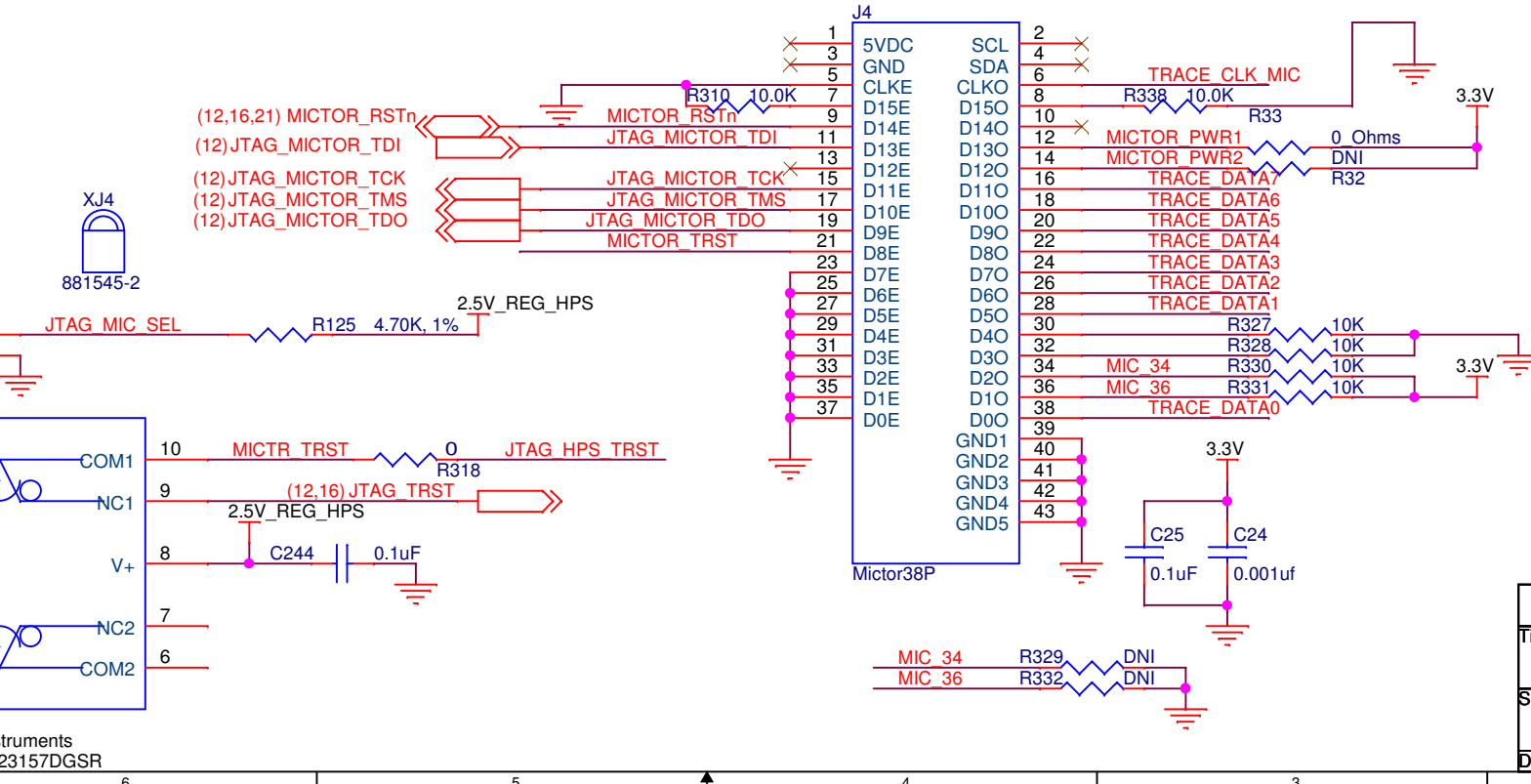
ENET_HPS_RX_CLK ↔ ENET_HPS_RX_CLK (18)
 ENET_HPS_RX_DV ↔ ENET_HPS_RX_DV (18)
 ENET_HPS_MDIO ↔ ENET_HPS_MDIO (18)
 ENET_HPS_INTn ↔ ENET_HPS_INTn (18)

HPS_RESETn ↔ HPS_RESETn (16,21)

USER_LED_HPS[3..0] ↔ USER_LED_HPS[3..0] (23)

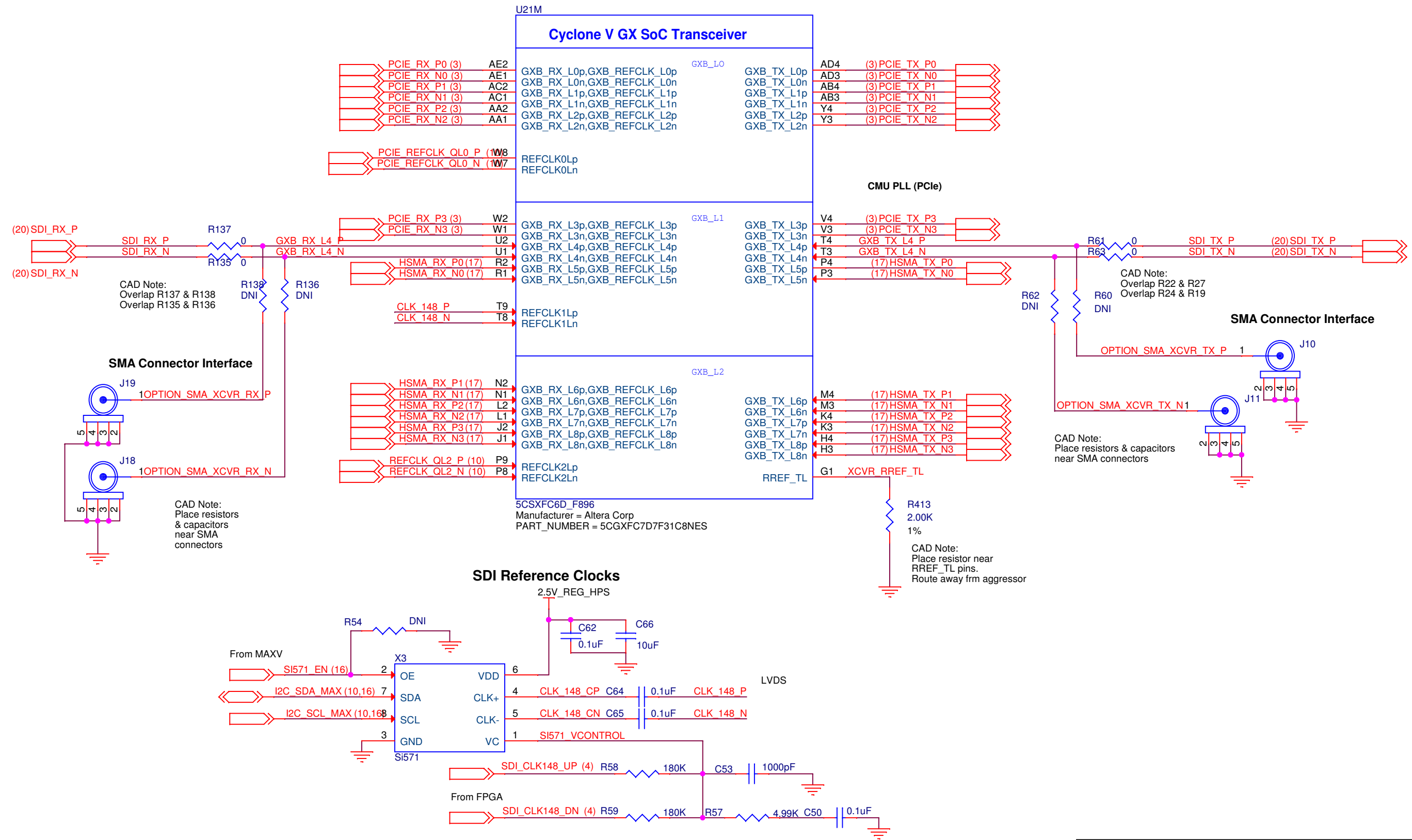


5CSXFC6D_F896
 Manufacturer = Altera Corp
 PART_NUMBER = 5CGXFC7D7F31C8NES



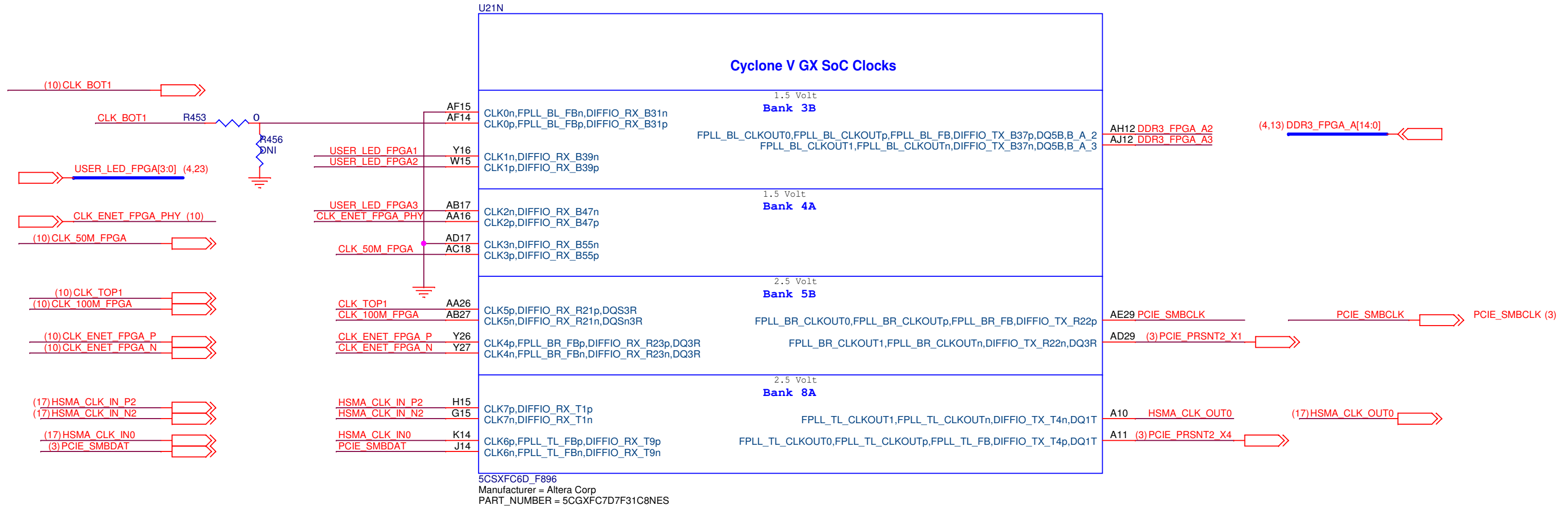
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Cyclone V GX SoC Transceivers and Power



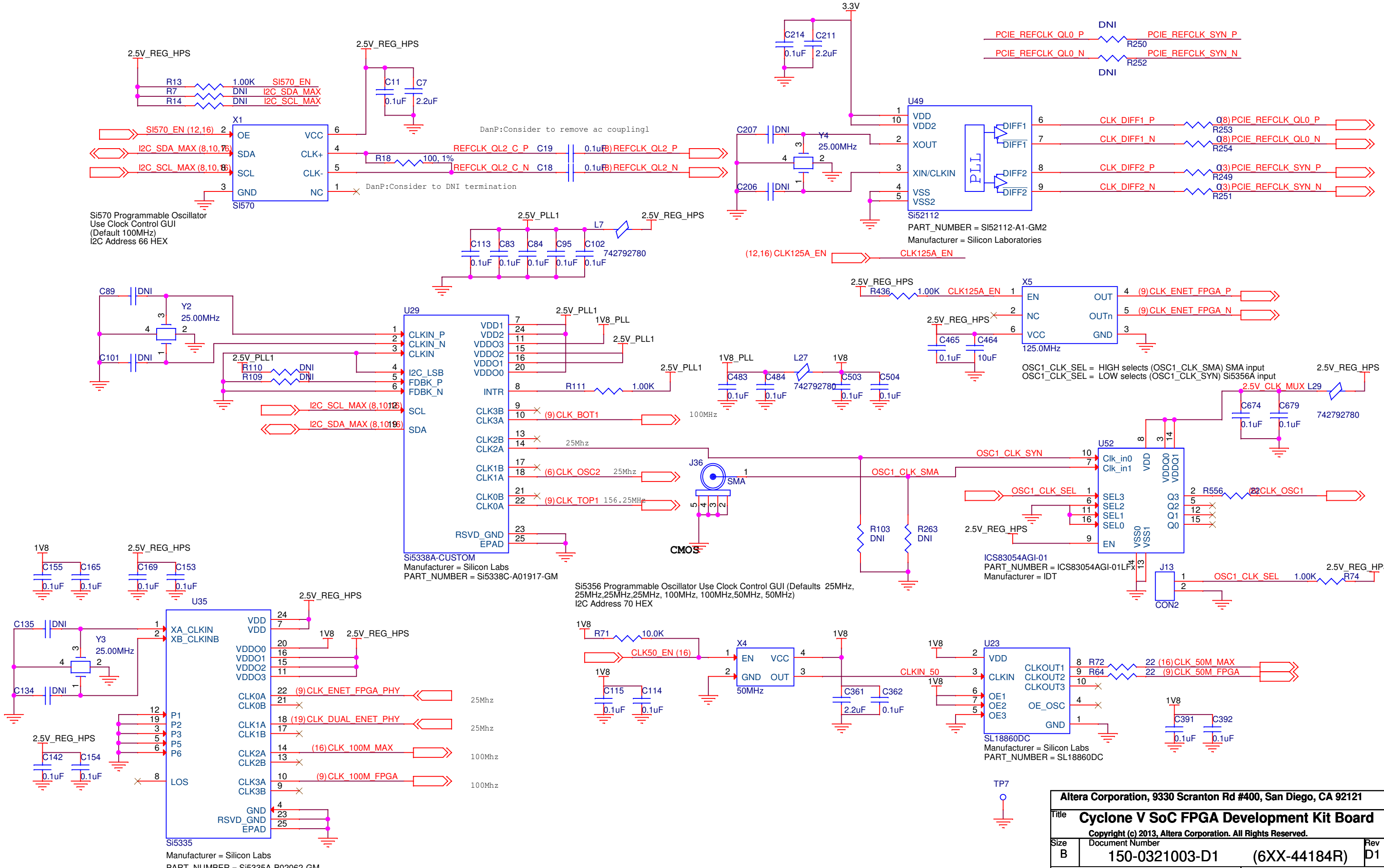
Cyclone V GX SoC Clocks

HSMA CLK IN P2 R412 100, 1% HSMA CLK IN N2



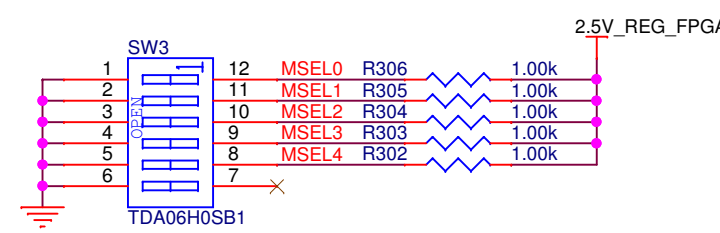
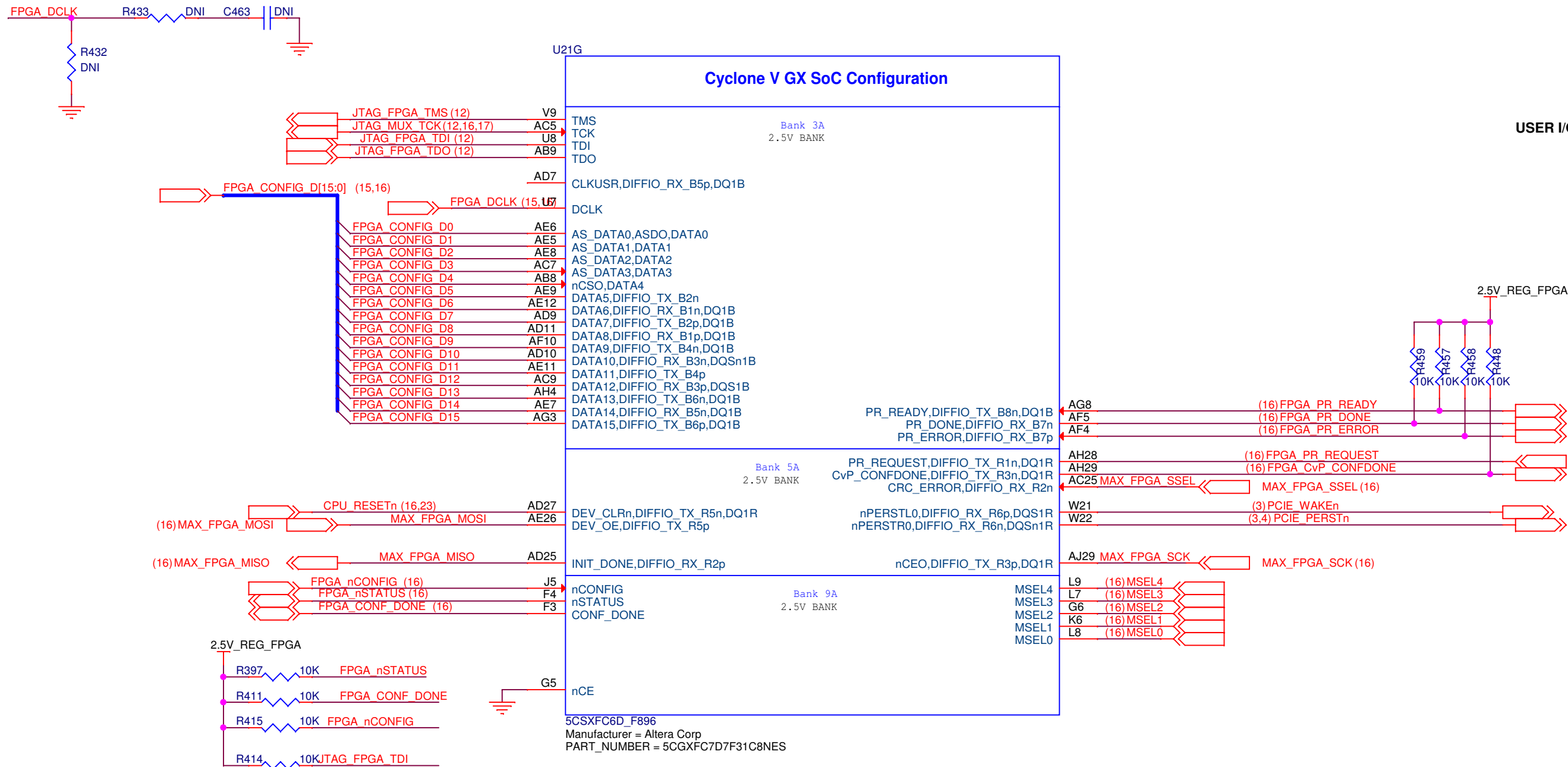
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PLL



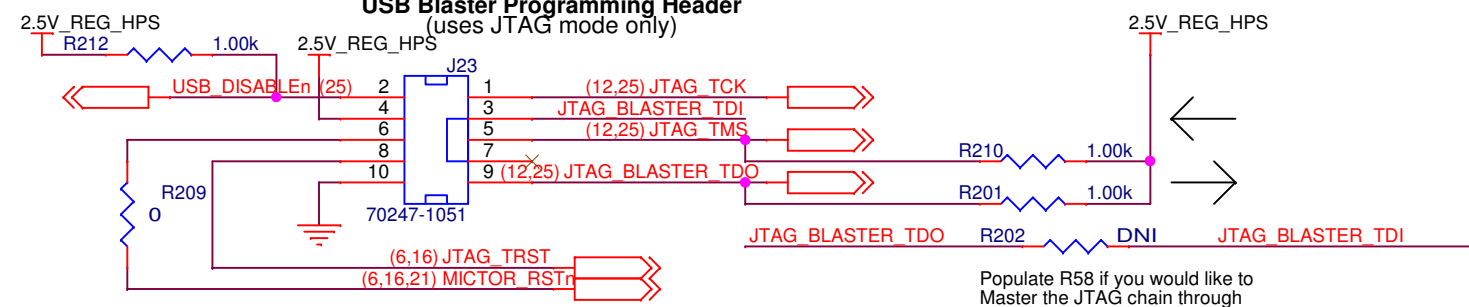
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Cyclone V GX SoC Configuration

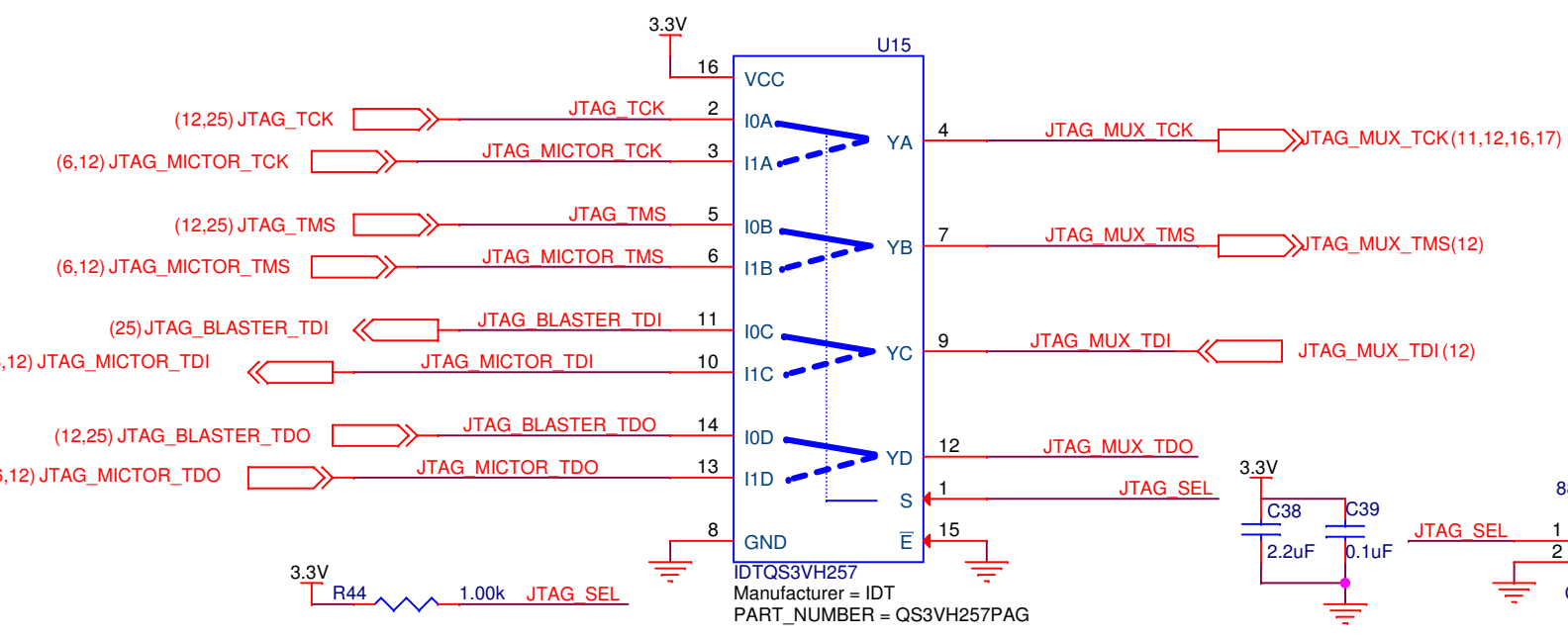
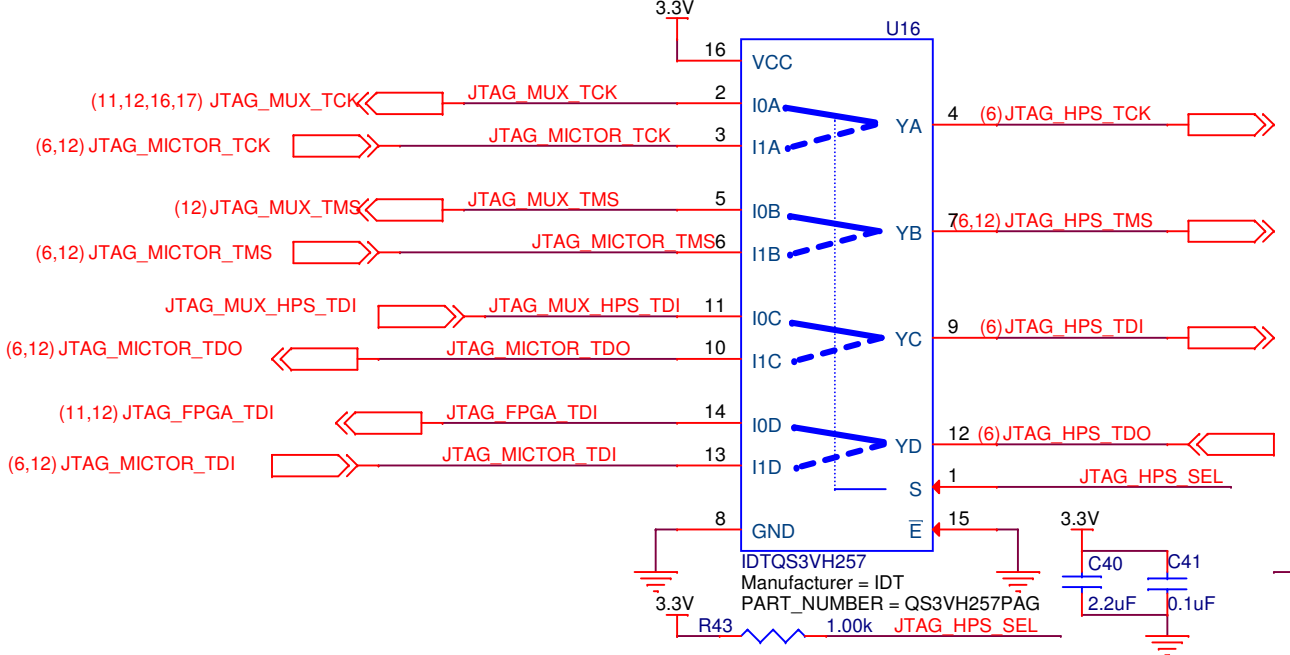
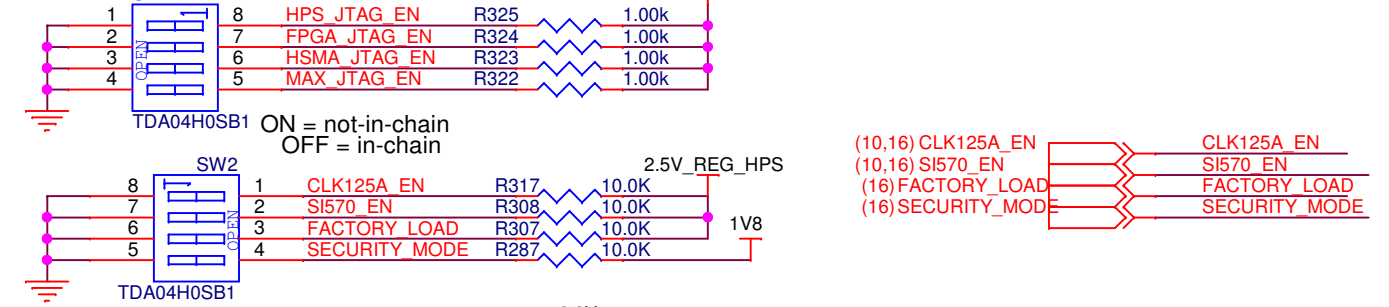


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USB Blaster Programming Header (uses JTAG mode only)



JTAG Chain Control



JTAG

Logic 0 = pin 10 <-> pin 9 (HPS Bypass)
Logic 1 = pin 10 <-> pin 2 (HPS Enable)

Logic 0 = pin 6 <-> pin 7 (HPS Bypass)
Logic 1 = pin 6 <-> pin 4 (HPS Enable)

Logic 0 = pin 10 <-> pin 9 (FPGA Bypass)
Logic 1 = pin 10 <-> pin 2 (FPGA Enable)

Logic 0 = pin 6 <-> pin 7 (FPGA Bypass)
Logic 1 = pin 6 <-> pin 4 (FPGA Enable)

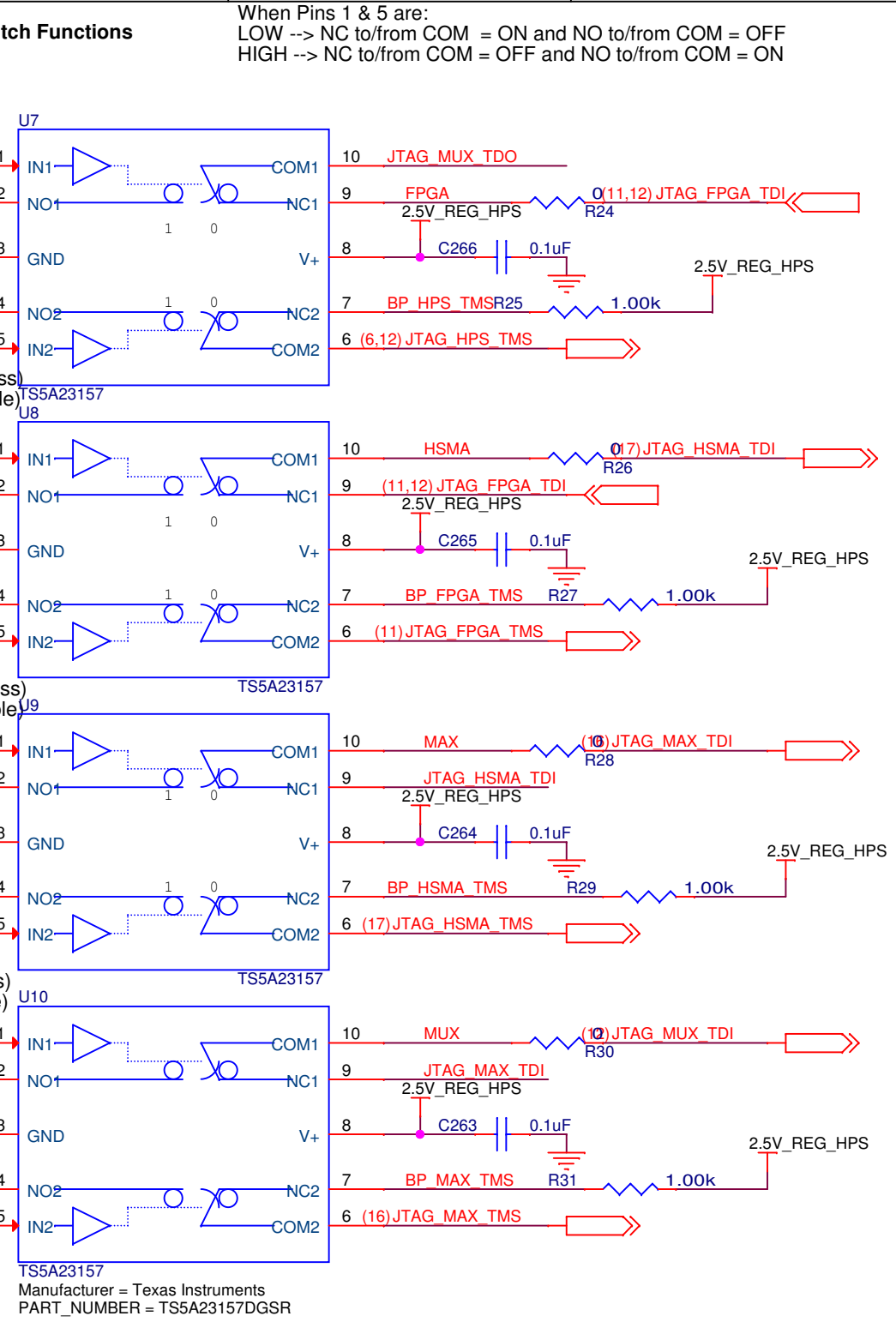
Logic 0 = pin 10 <-> pin 9 (HSMA Bypass)
Logic 1 = pin 10 <-> pin 2 (HSMA Enable)

Logic 0 = pin 6 <-> pin 7 (HSMA Bypass)
Logic 1 = pin 6 <-> pin 4 (HSMA Enable)

Logic 0 = pin 10 <-> pin 9 (MAX II Bypass)
Logic 1 = pin 10 <-> pin 2 (MAX II Enable)

Logic 0 = pin 6 <-> pin 7 (HSMB Bypass)
Logic 1 = pin 6 <-> pin 4 (HSMB Enable)

TS5A23157 Switch Functions

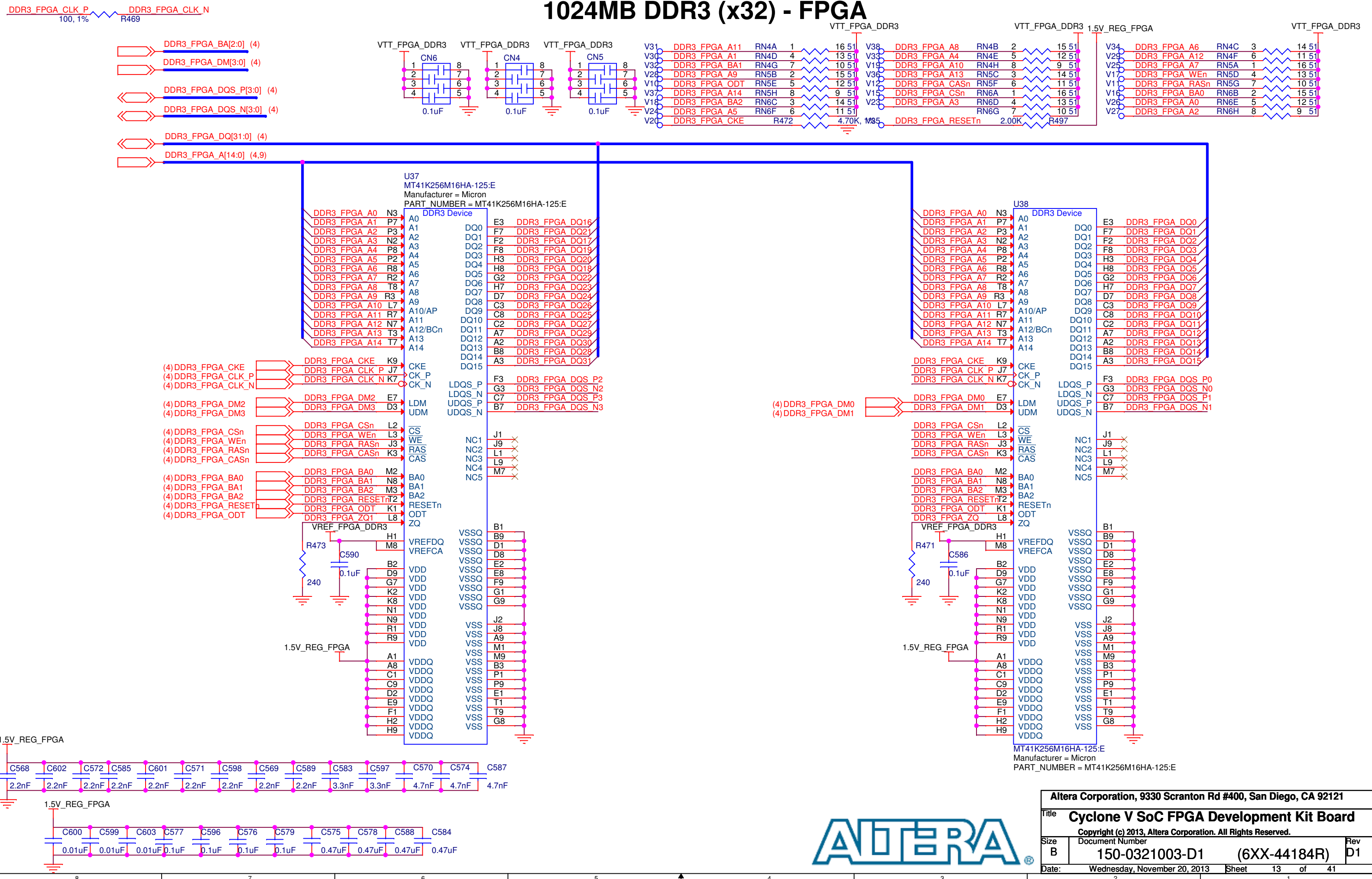


When Pins 1 & 5 are:
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

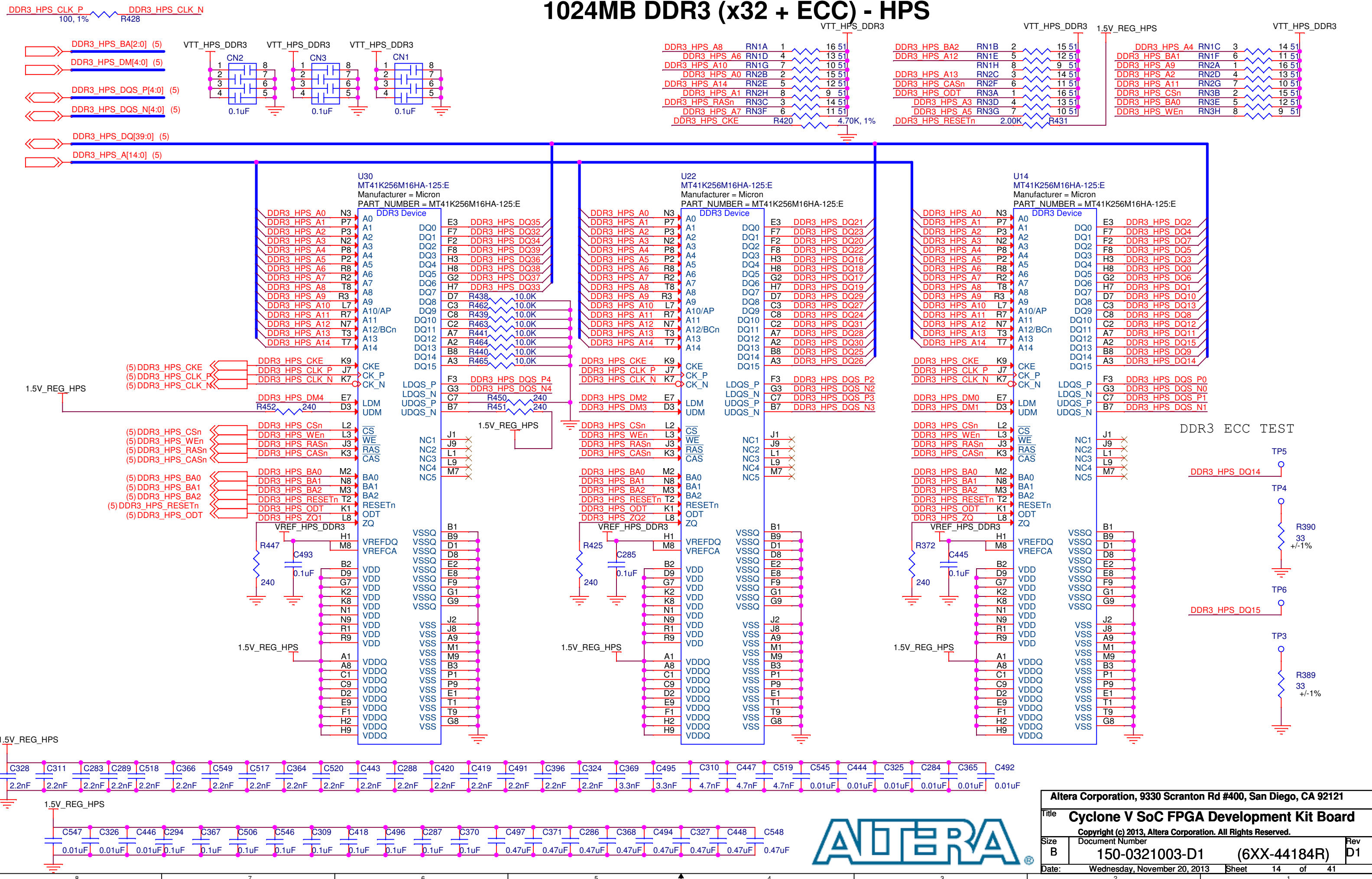


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1024MB DDR3 (x32) - FPGA



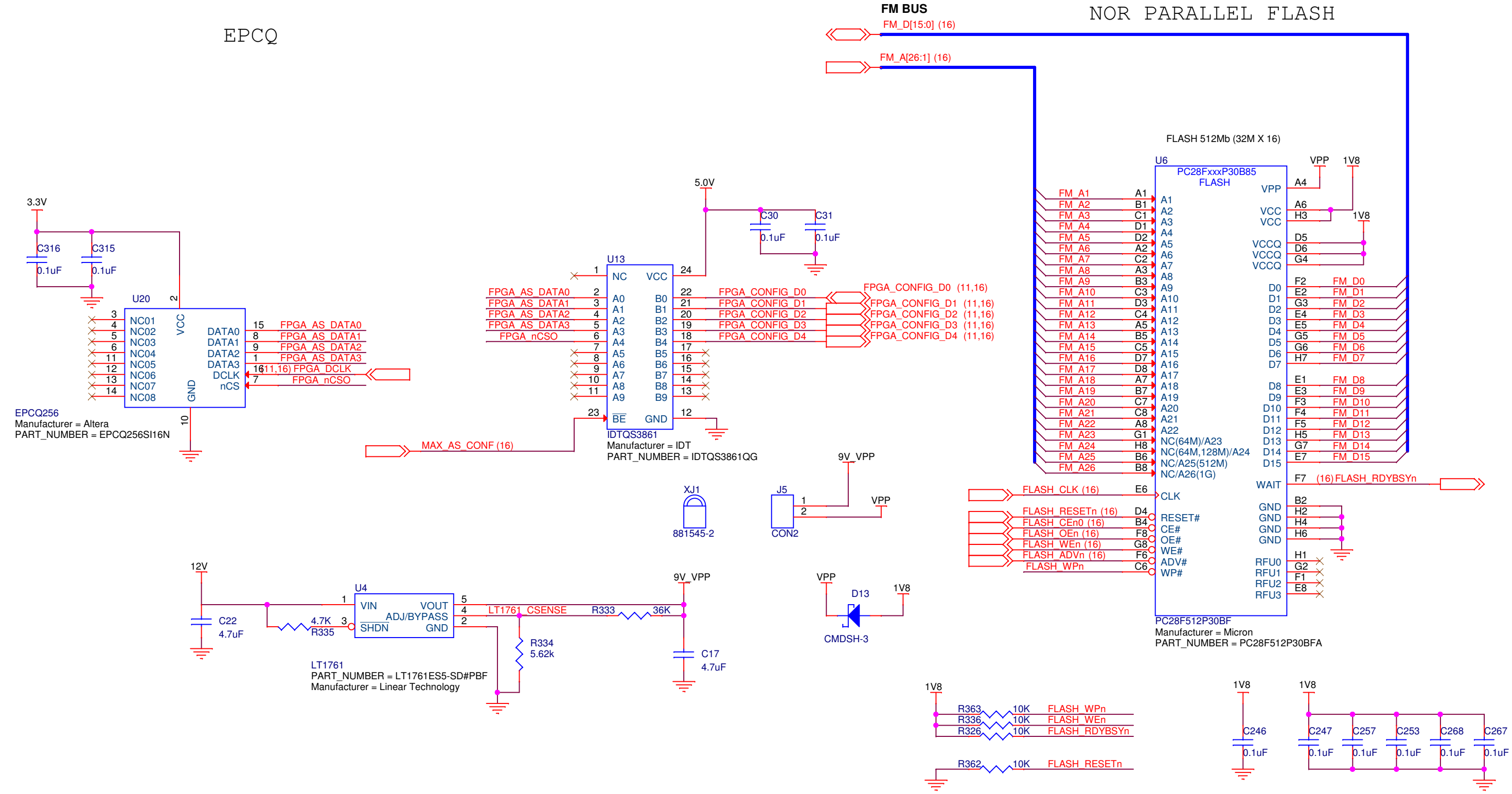
1024MB DDR3 (x32 + ECC) - HPS



FLASH, EPCQ

NOR PARALLEL FLASH

EPCQ

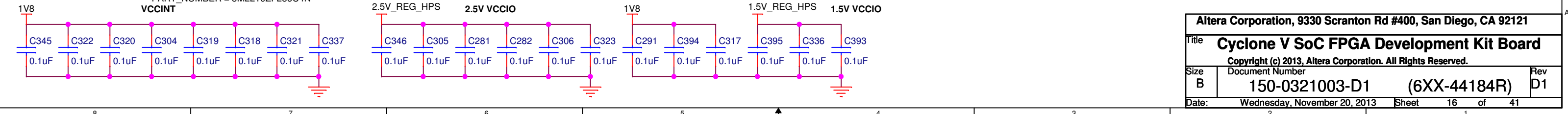
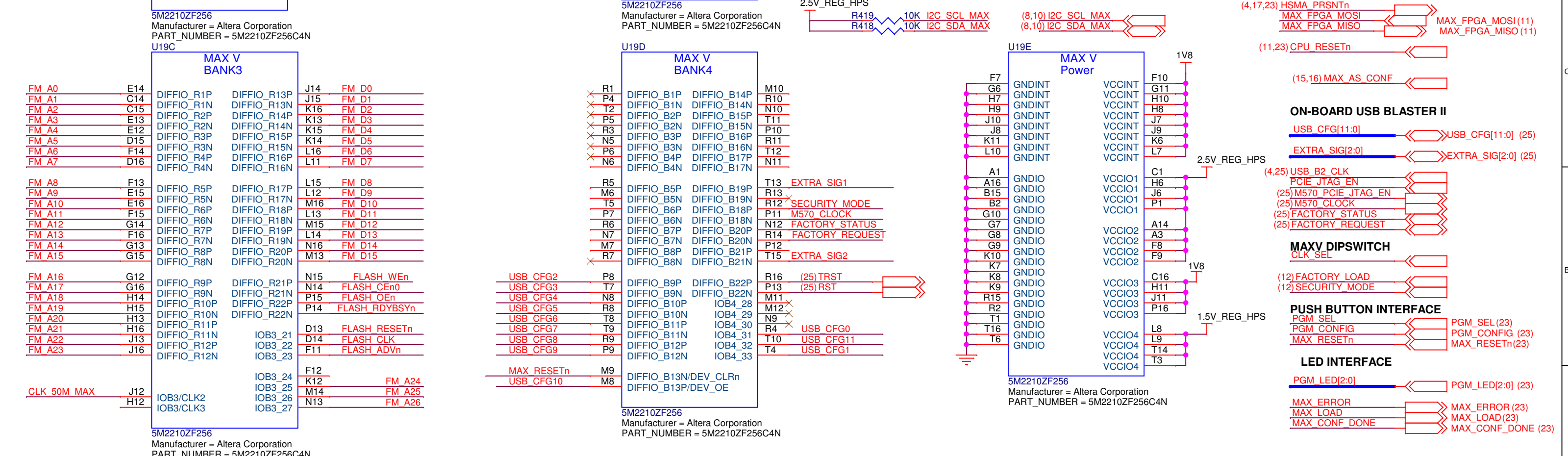
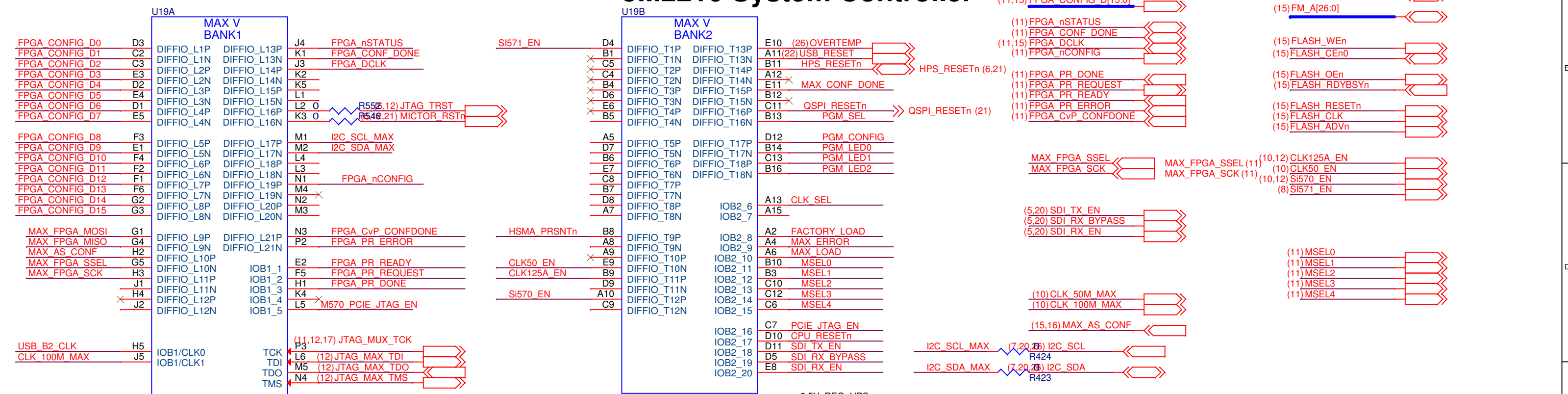


- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.



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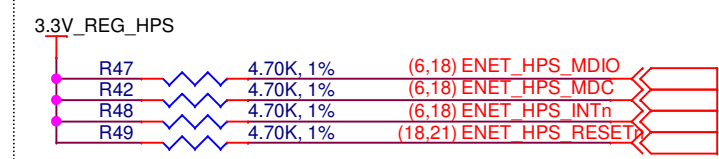
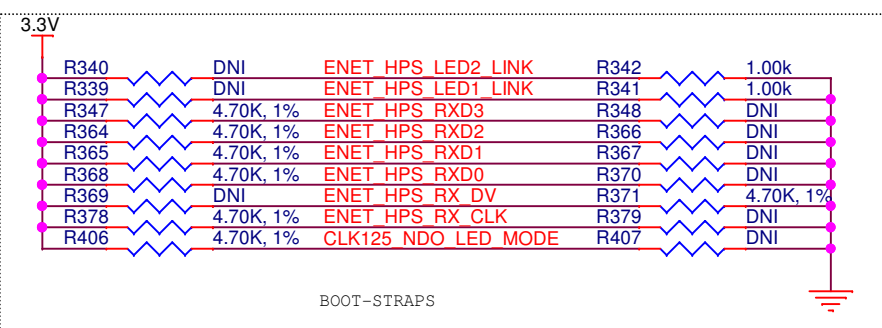
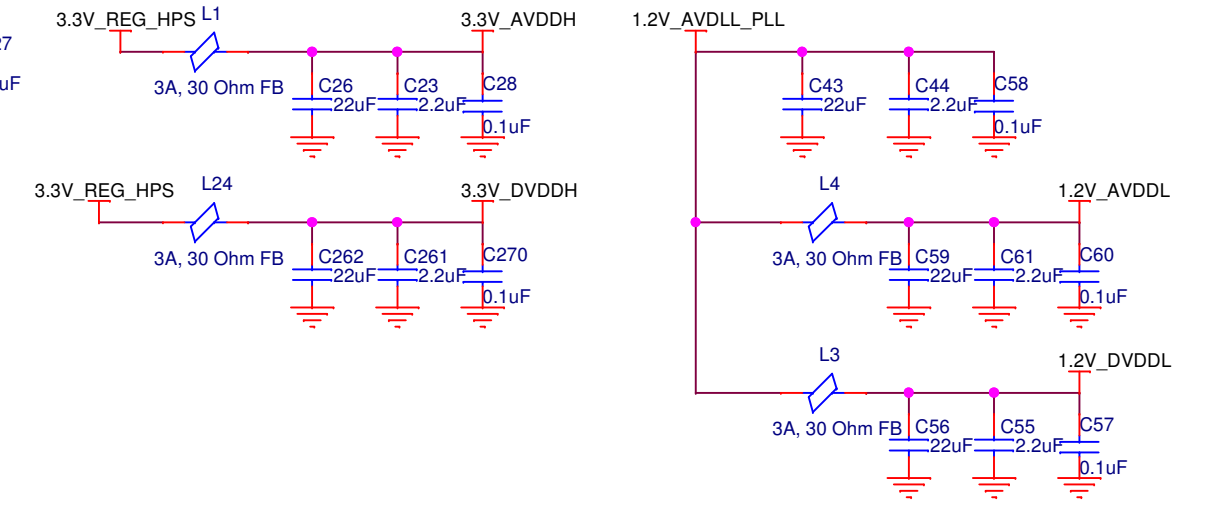
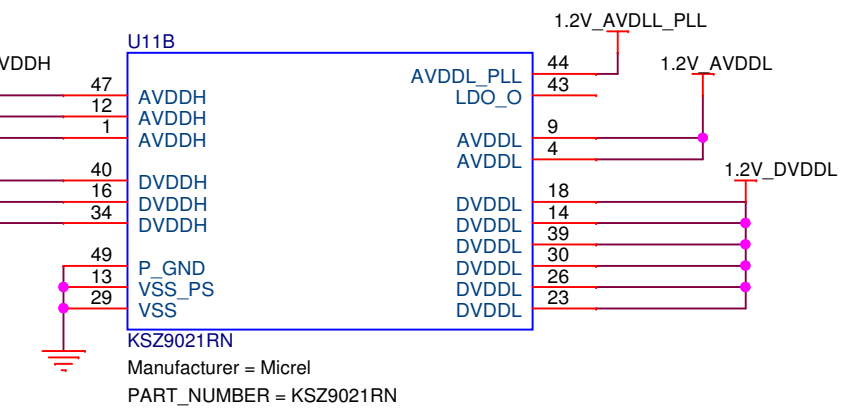
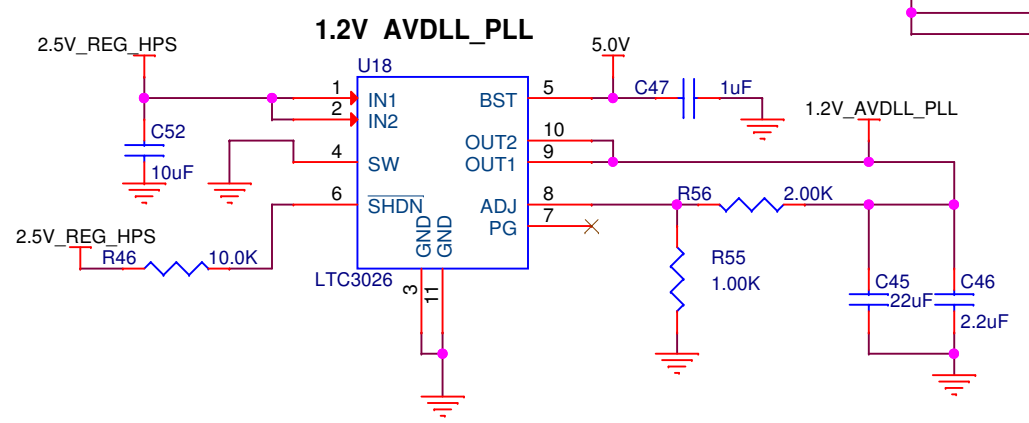
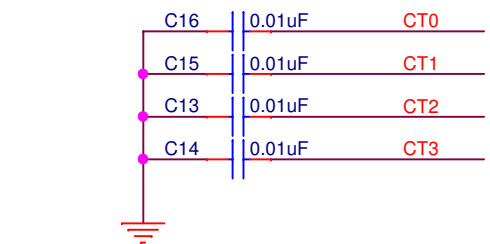
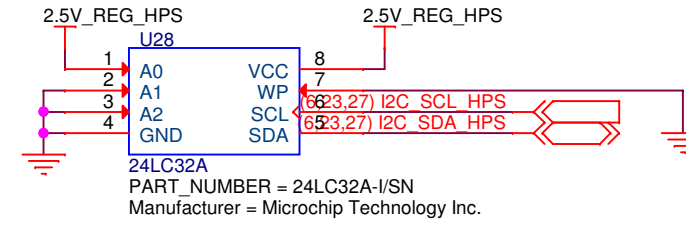
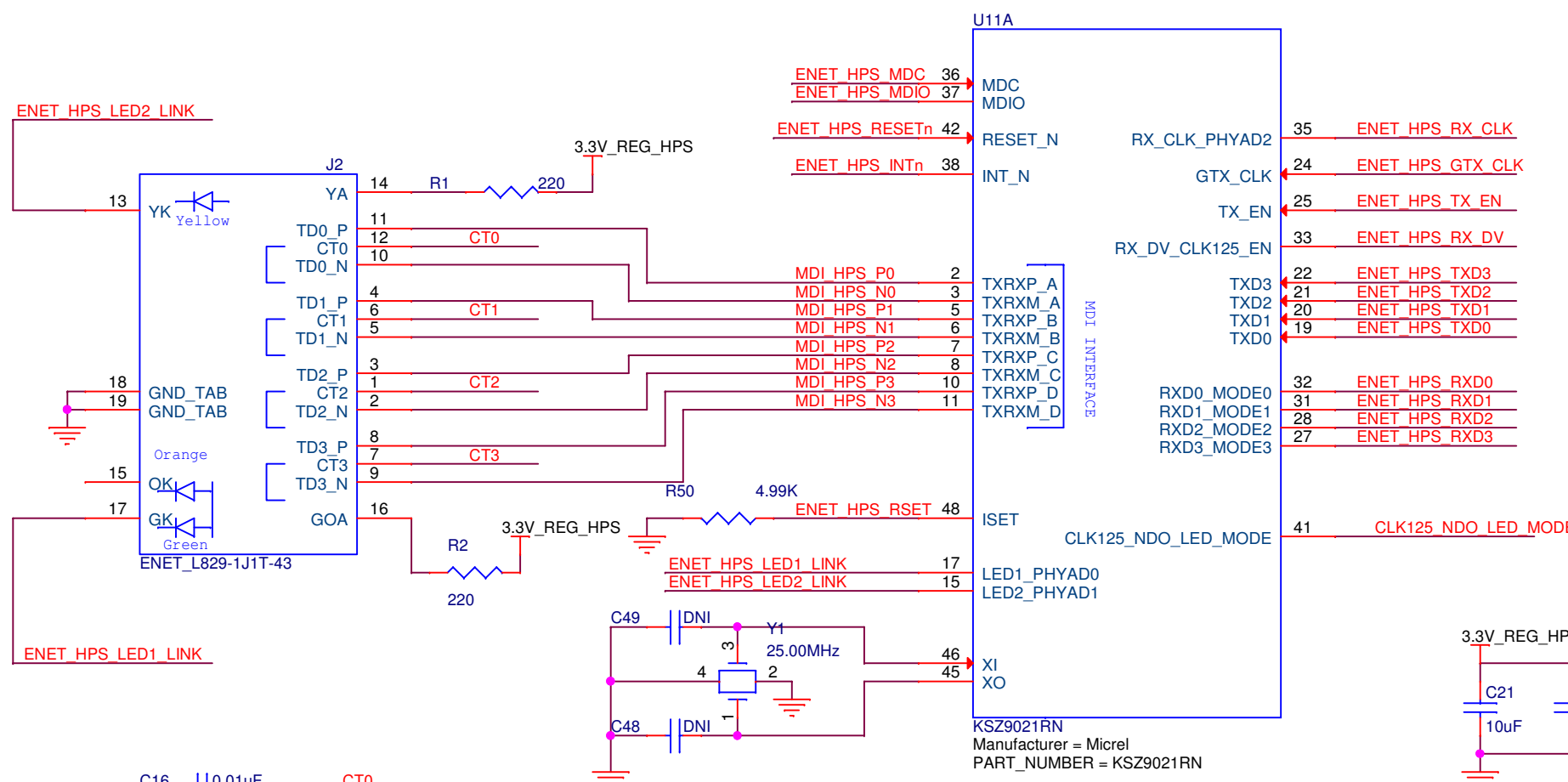
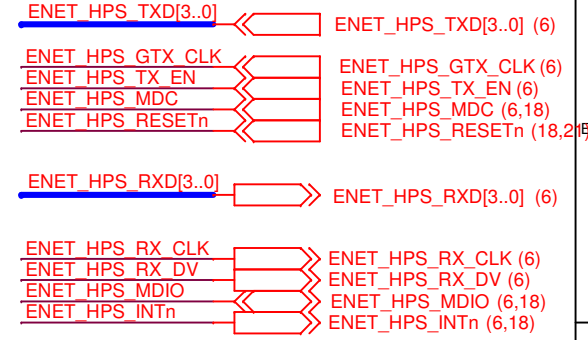
5M2210 System Controller



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Title Cyclone V SoC FPGA Development Kit Board			
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10/100/1000 Ethernet - HPS

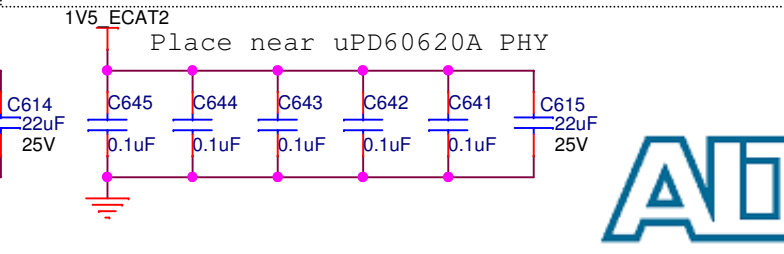
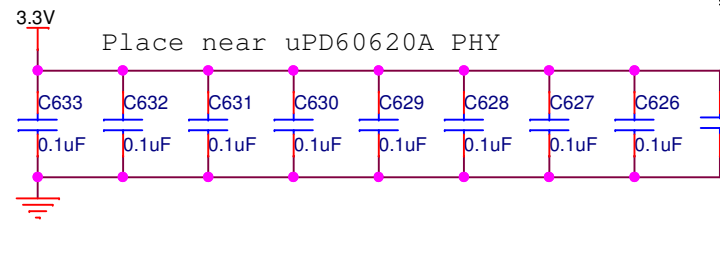
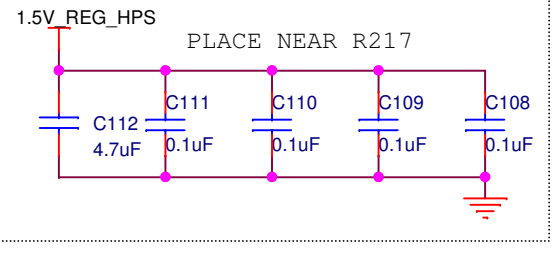
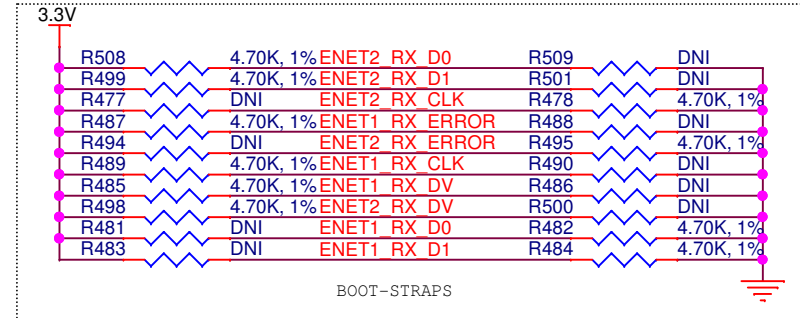
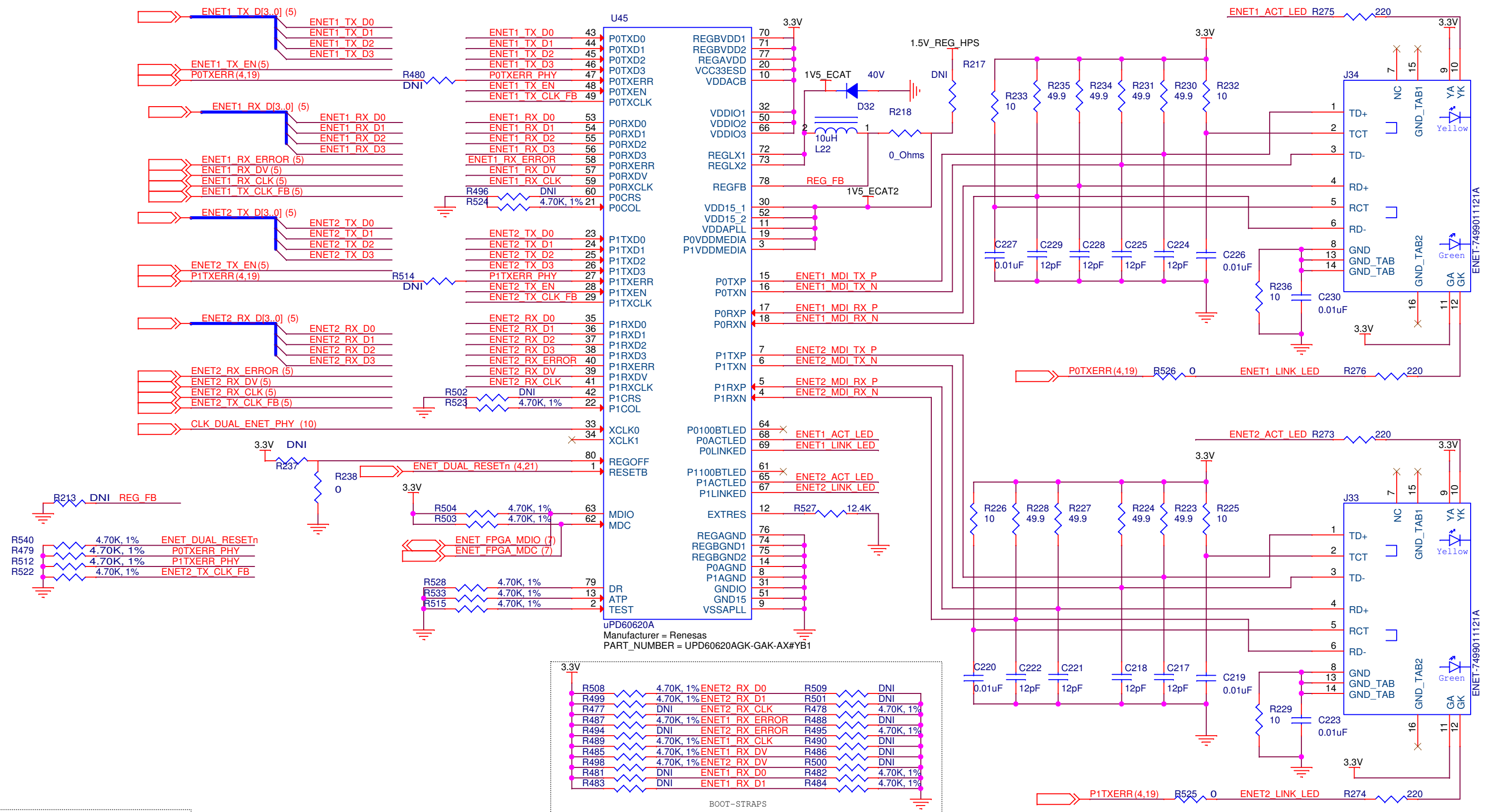
ETHERNET INTERFACE



Place near KSZ9021RN PHY



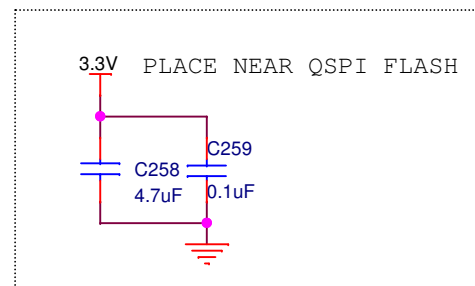
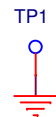
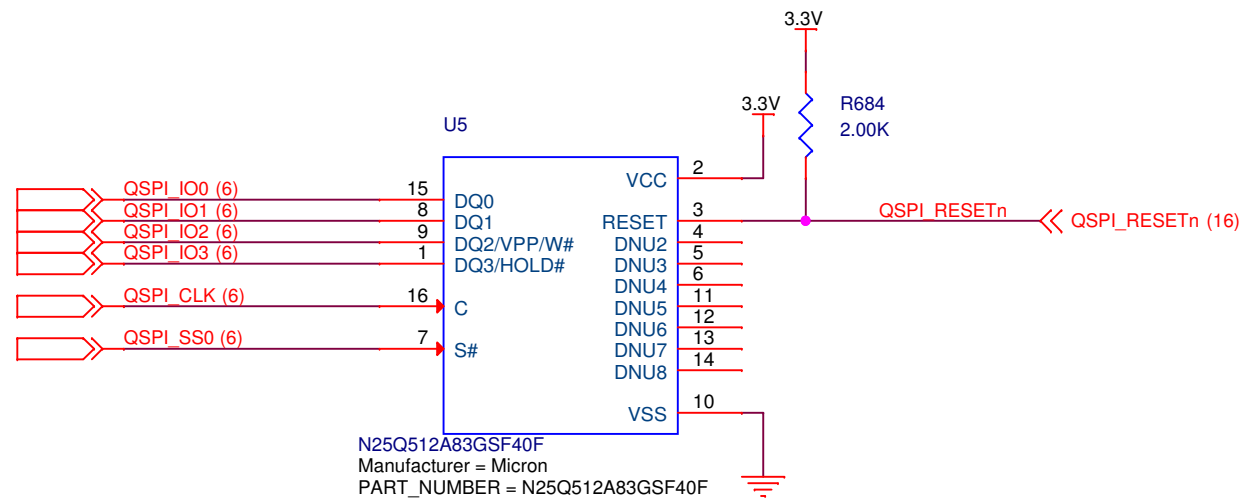
10/100M Ethernet - FPGA



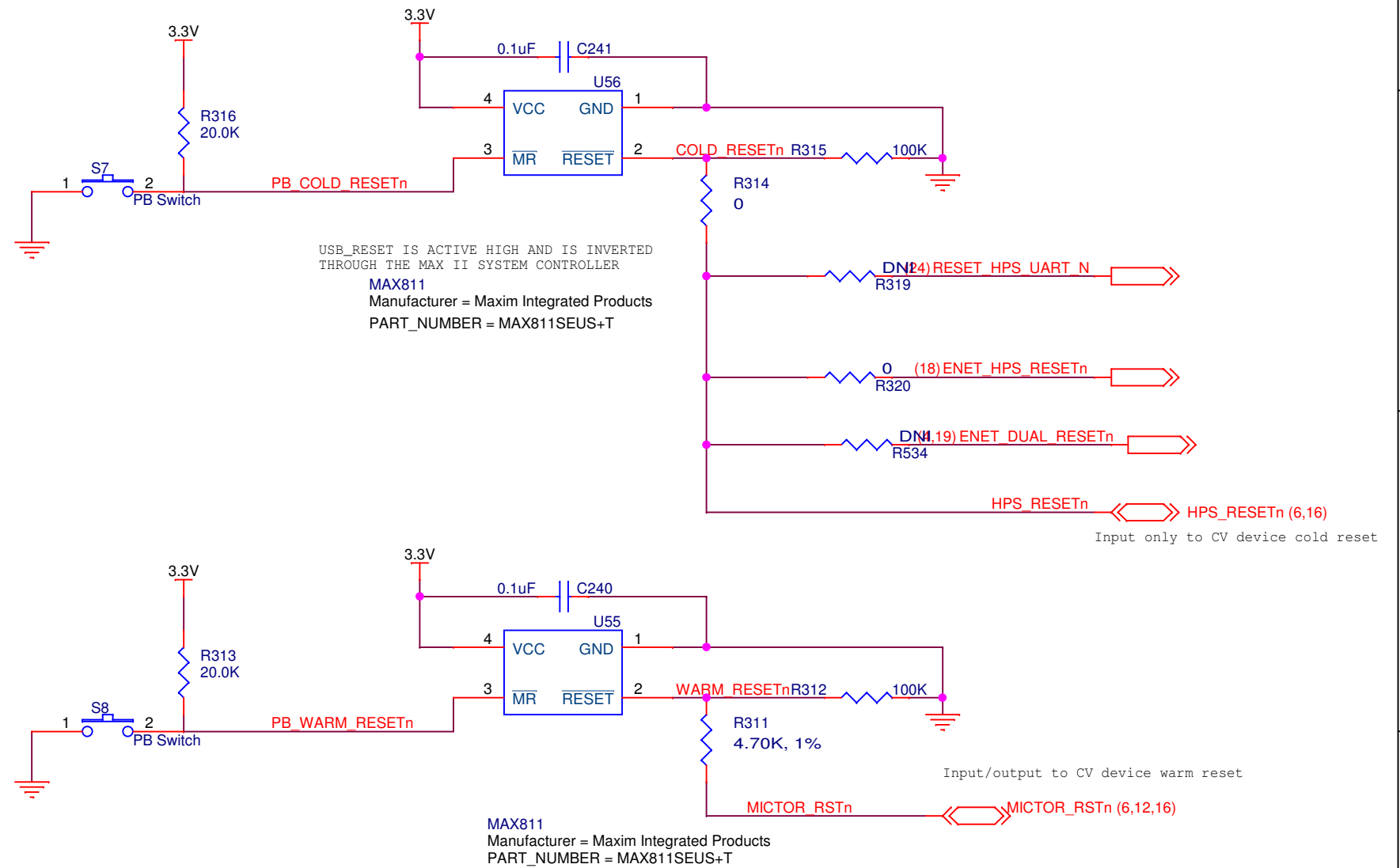
Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121			
Title Cyclone V SoC FPGA Development Kit Board			
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QSPI Flash & Reset Circuit

QSPI FLASH



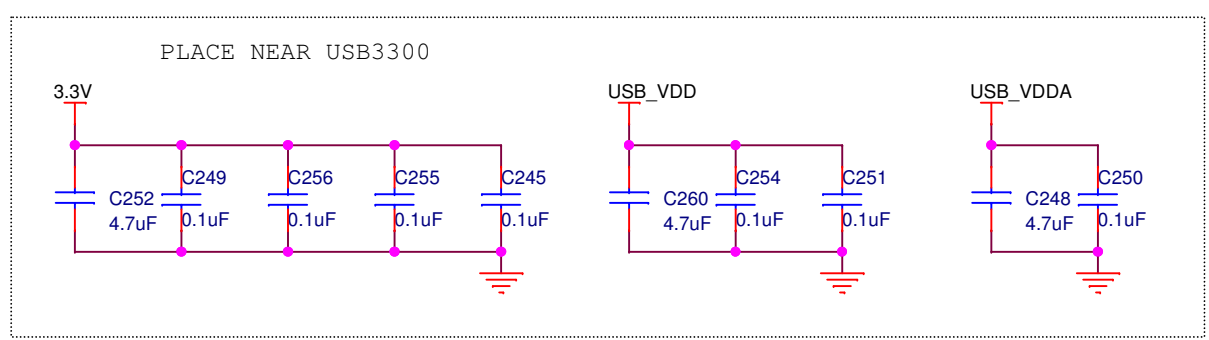
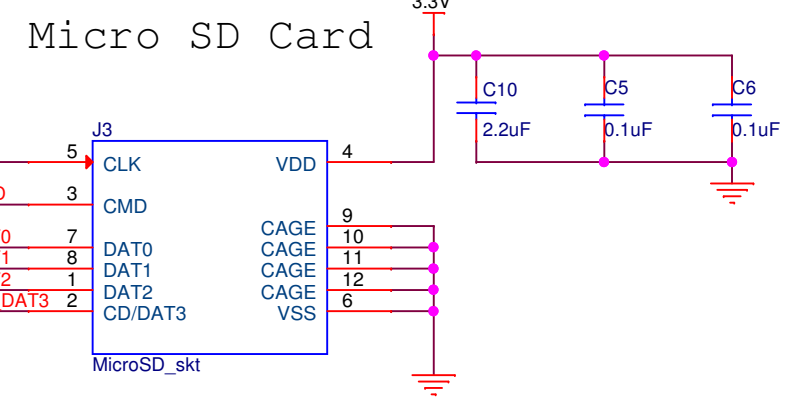
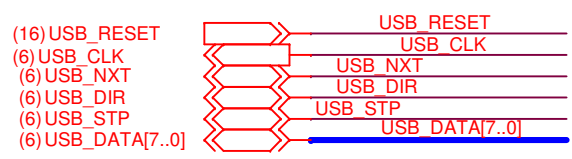
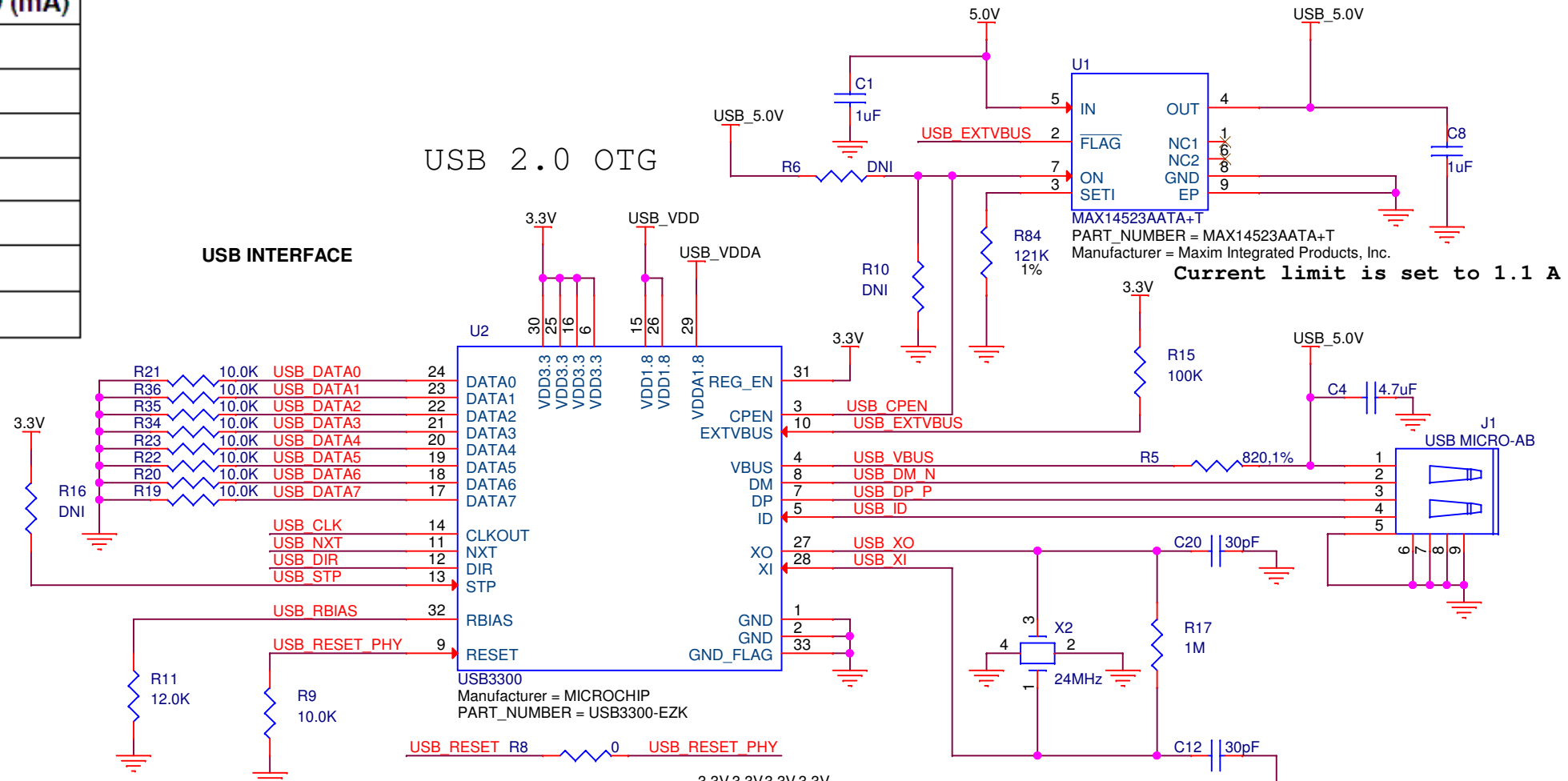
RESET CIRCUIT



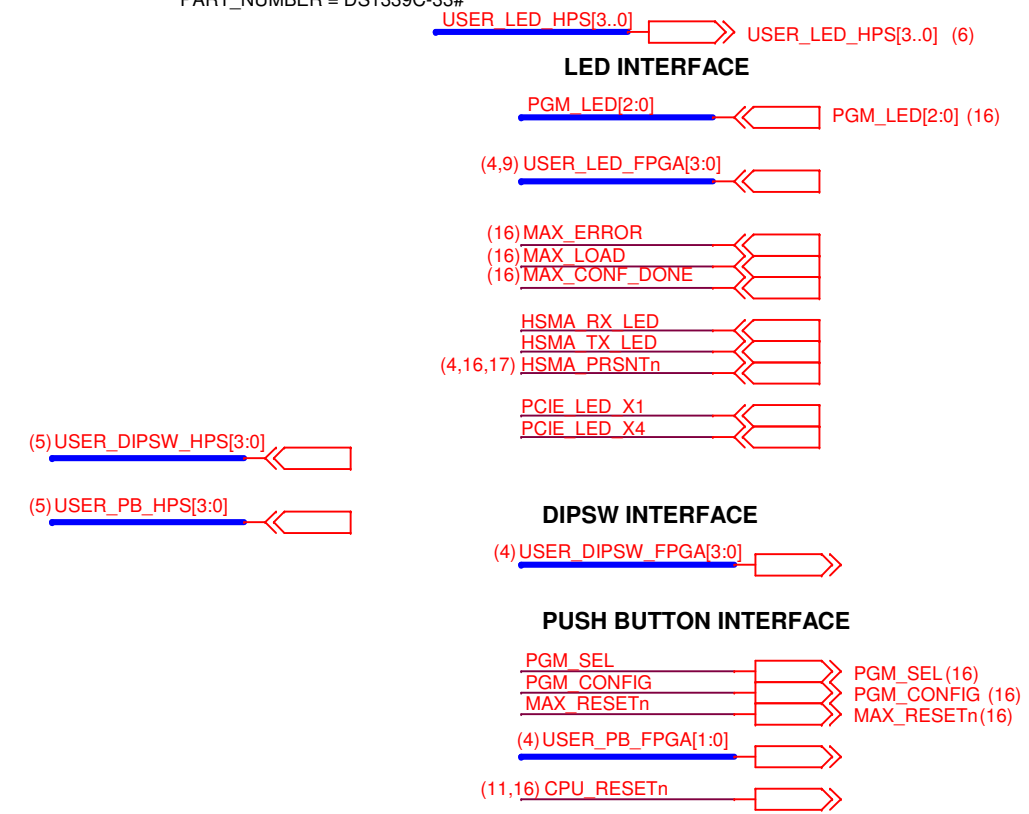
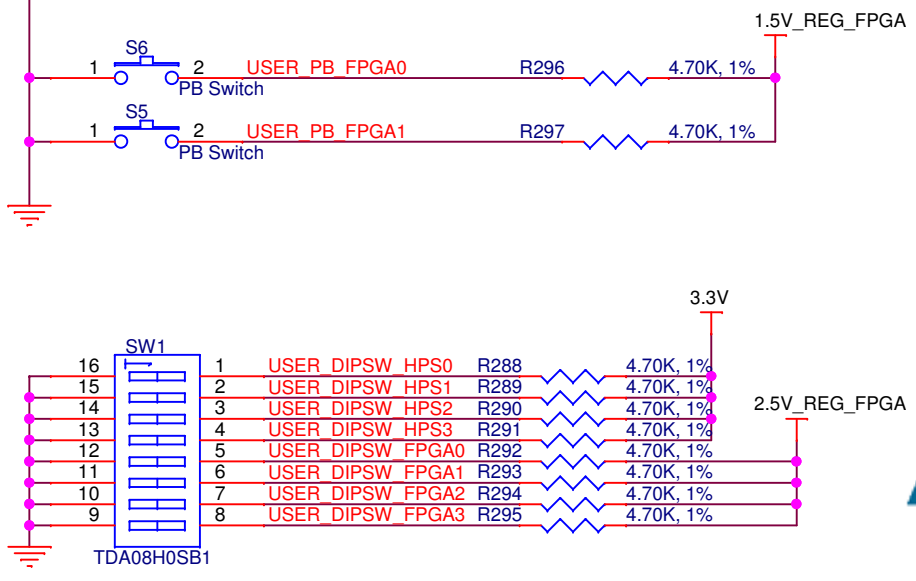
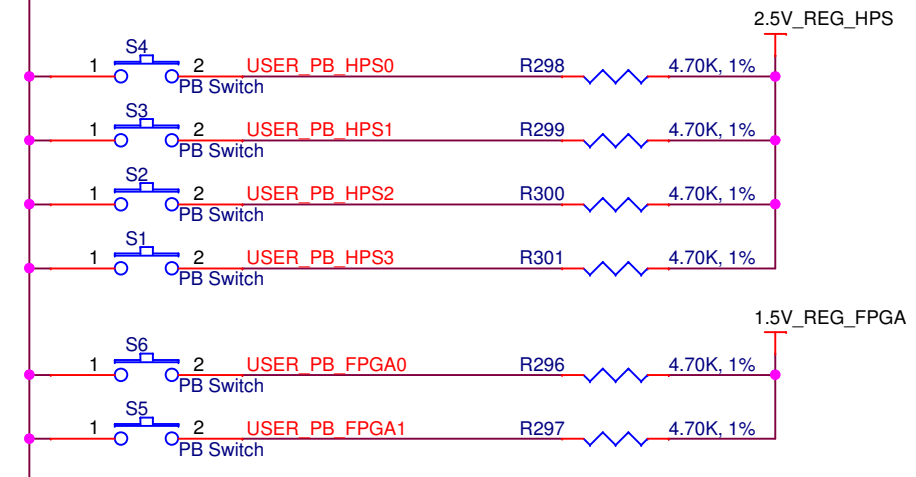
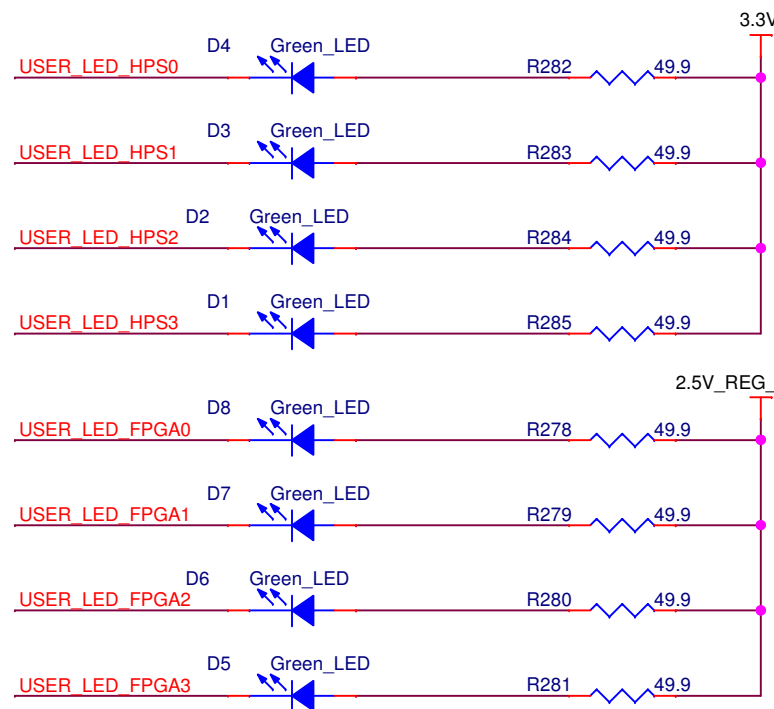
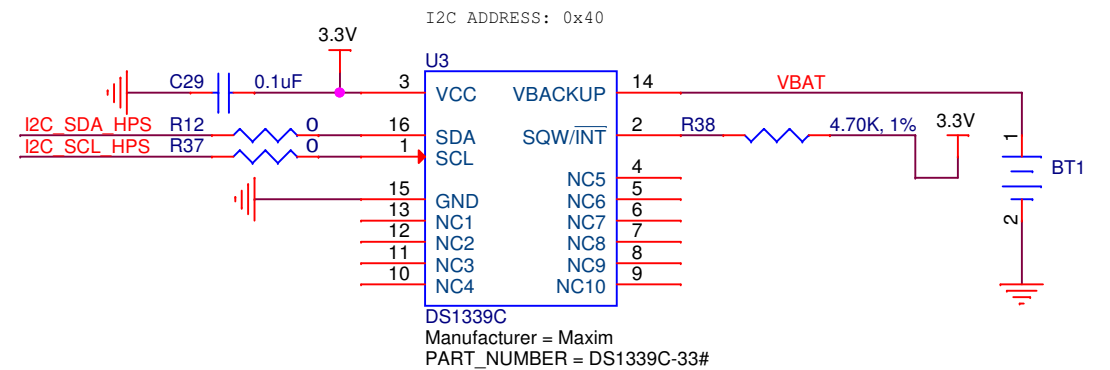
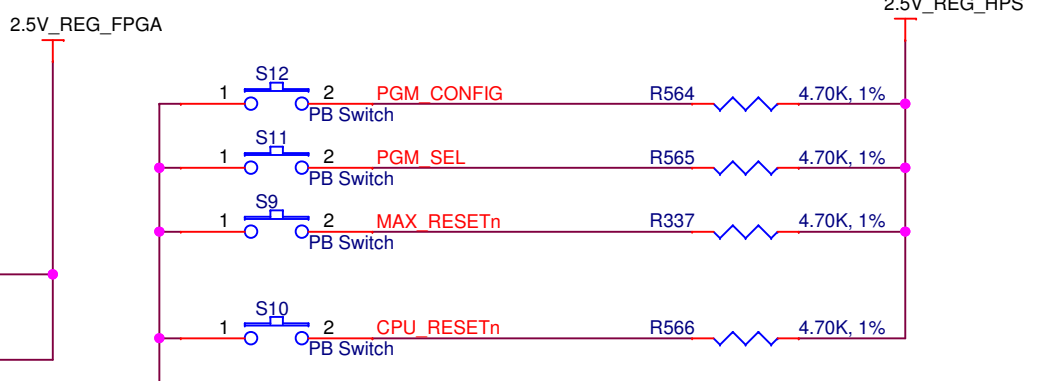
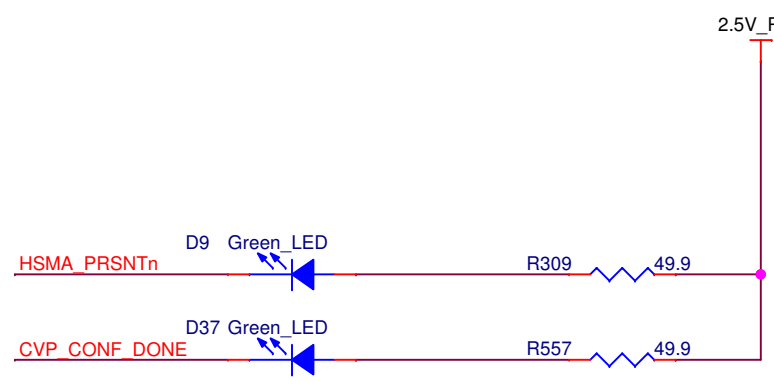
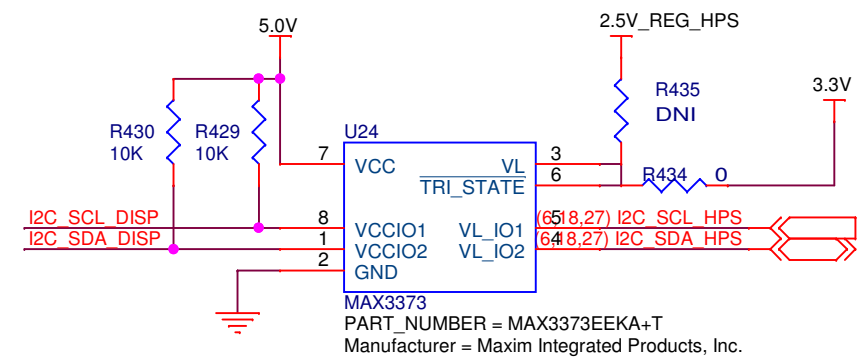
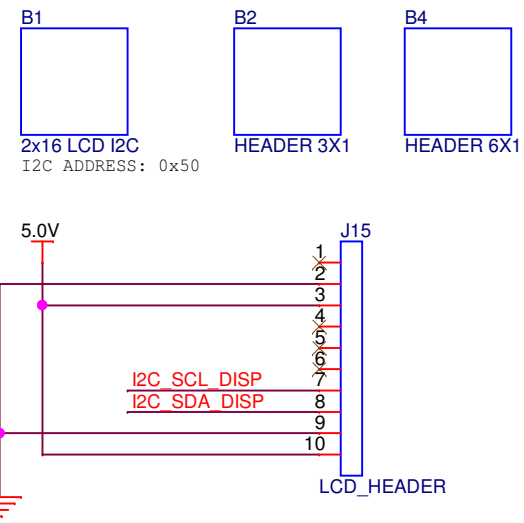
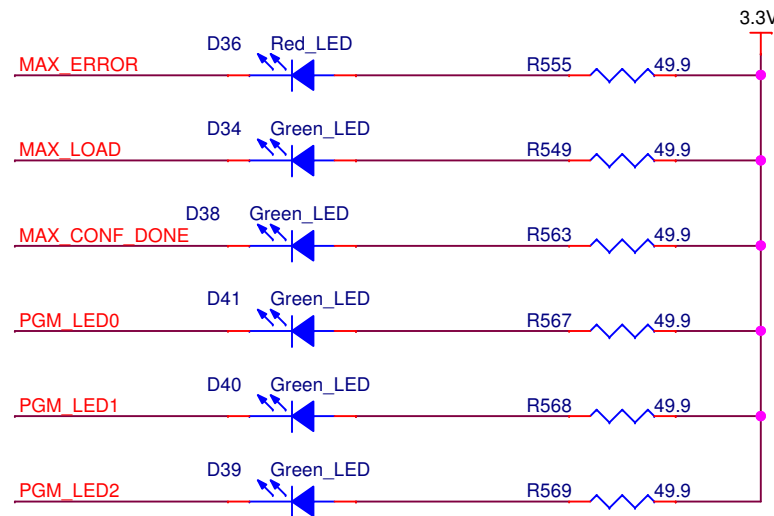
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USB 2.0 OTG , Micro SD Card

RSET1 (kΩ)	TYPICAL CURRENT LIMIT/THRESHOLD (mA)
91.78	1500
121	1145
221	632
301	466
422	333
563.12	250
∞ (Open)	0



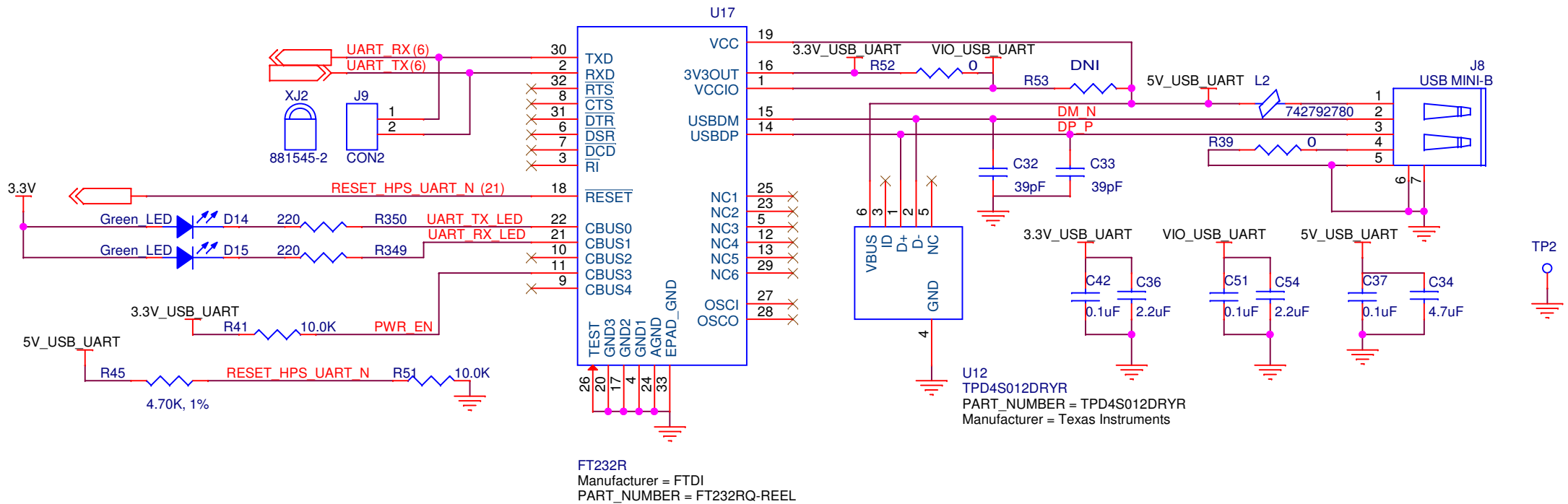
User I/O, RTC



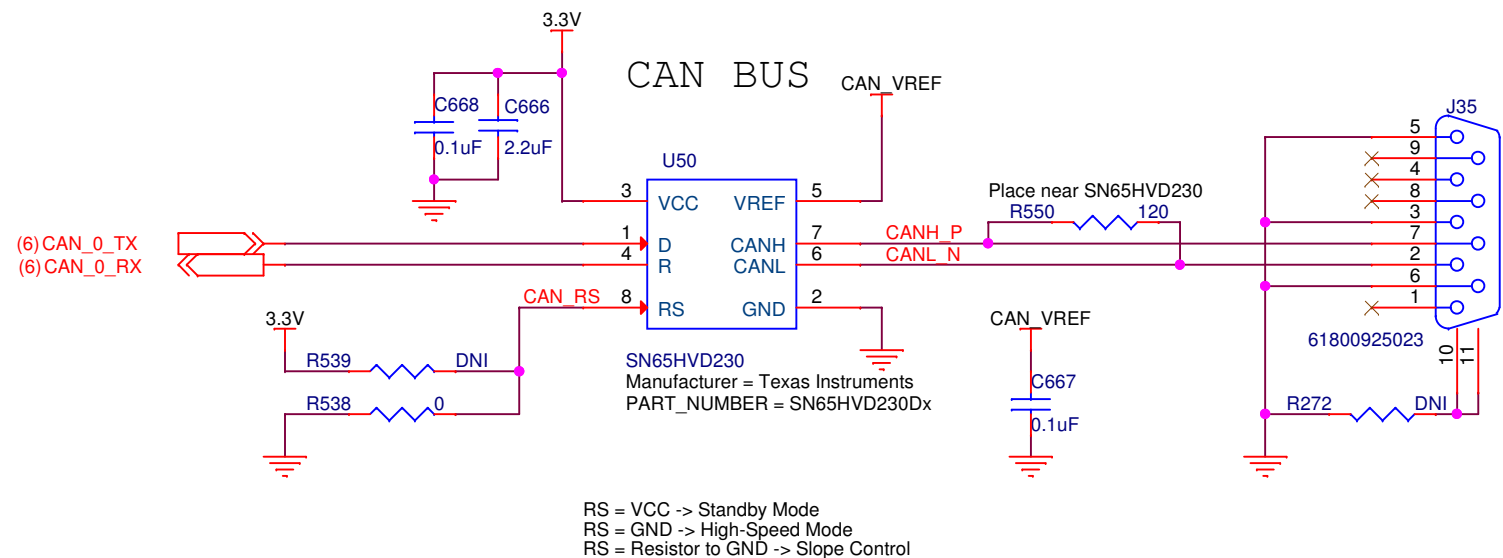
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UART, CAN

UART

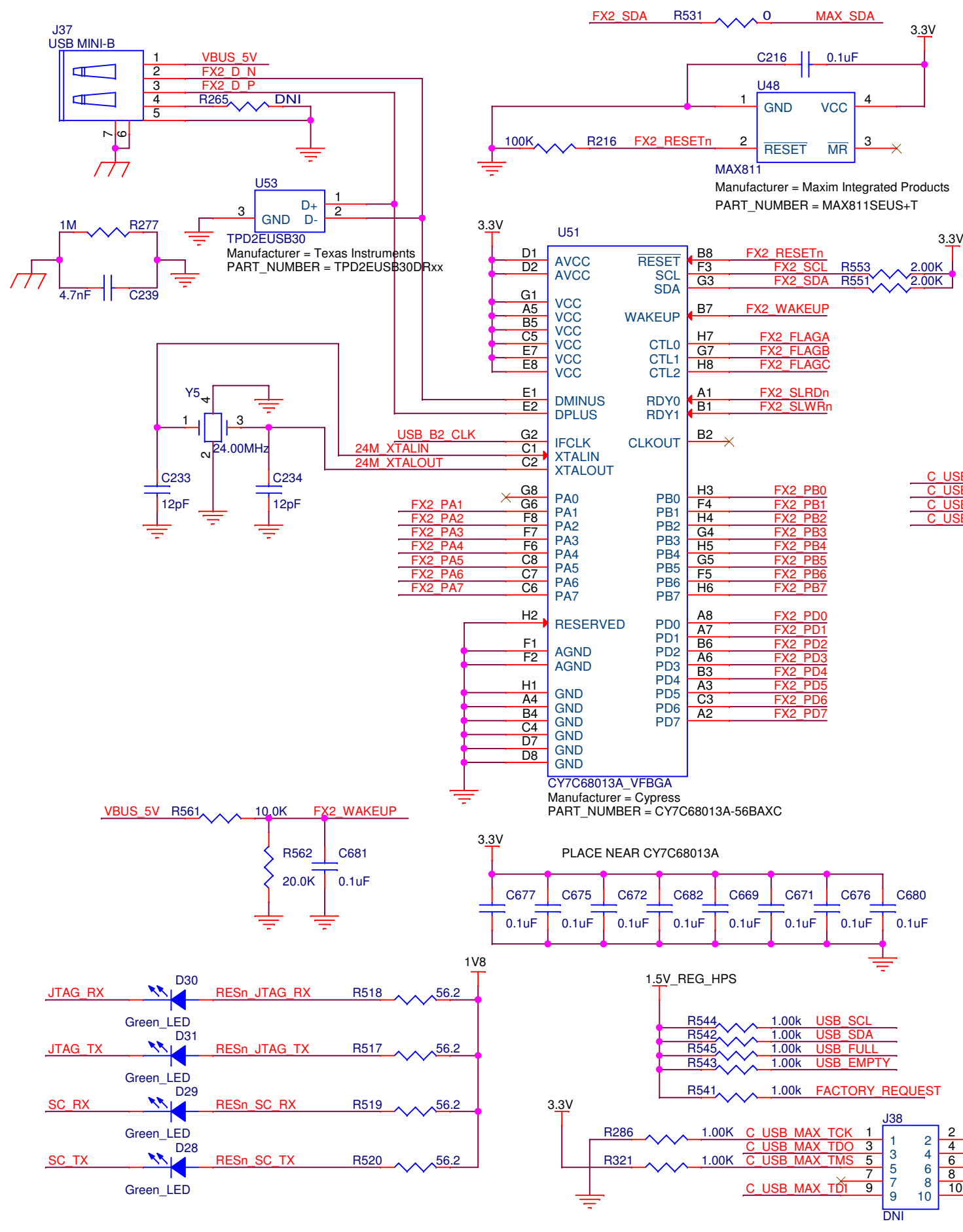


CAN BUS

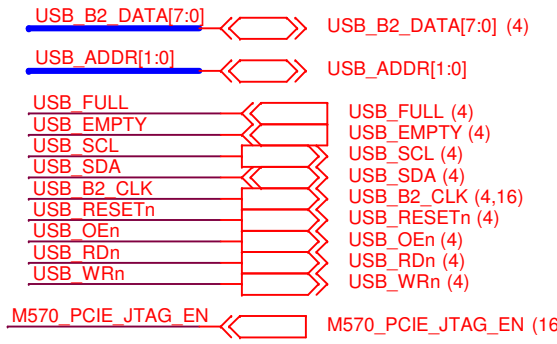


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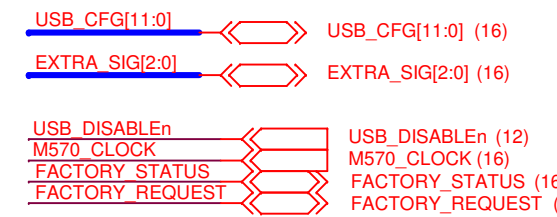
On-Board USB Blaster II



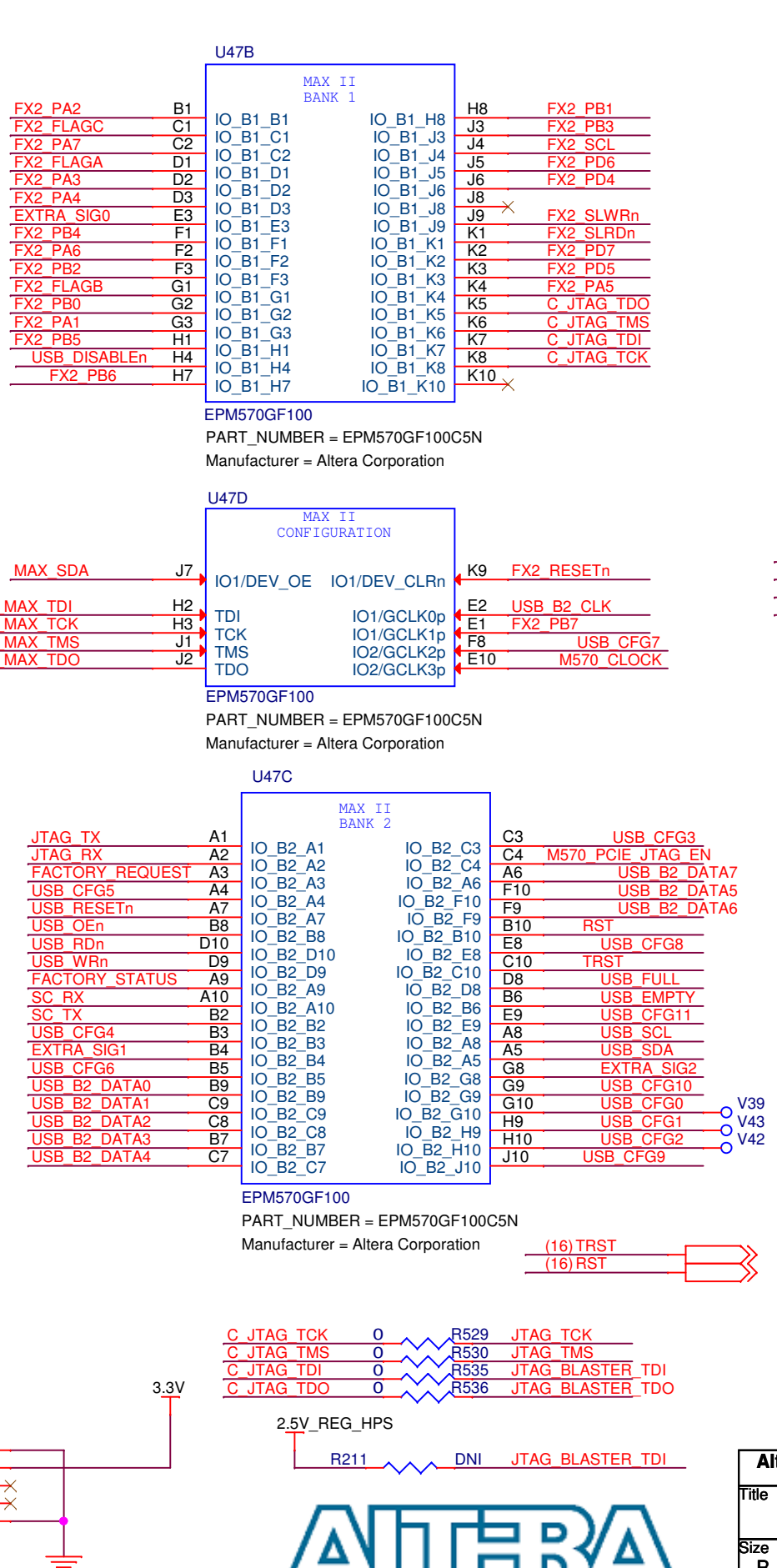
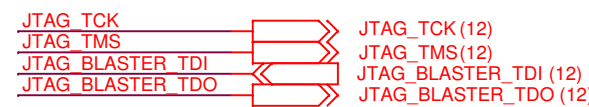
FPGA USB INTERFACE



MAX V USB INTERFACE



JTAG INTERFACE



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Title: **Cyclone V SoC FPGA Development Kit Board**

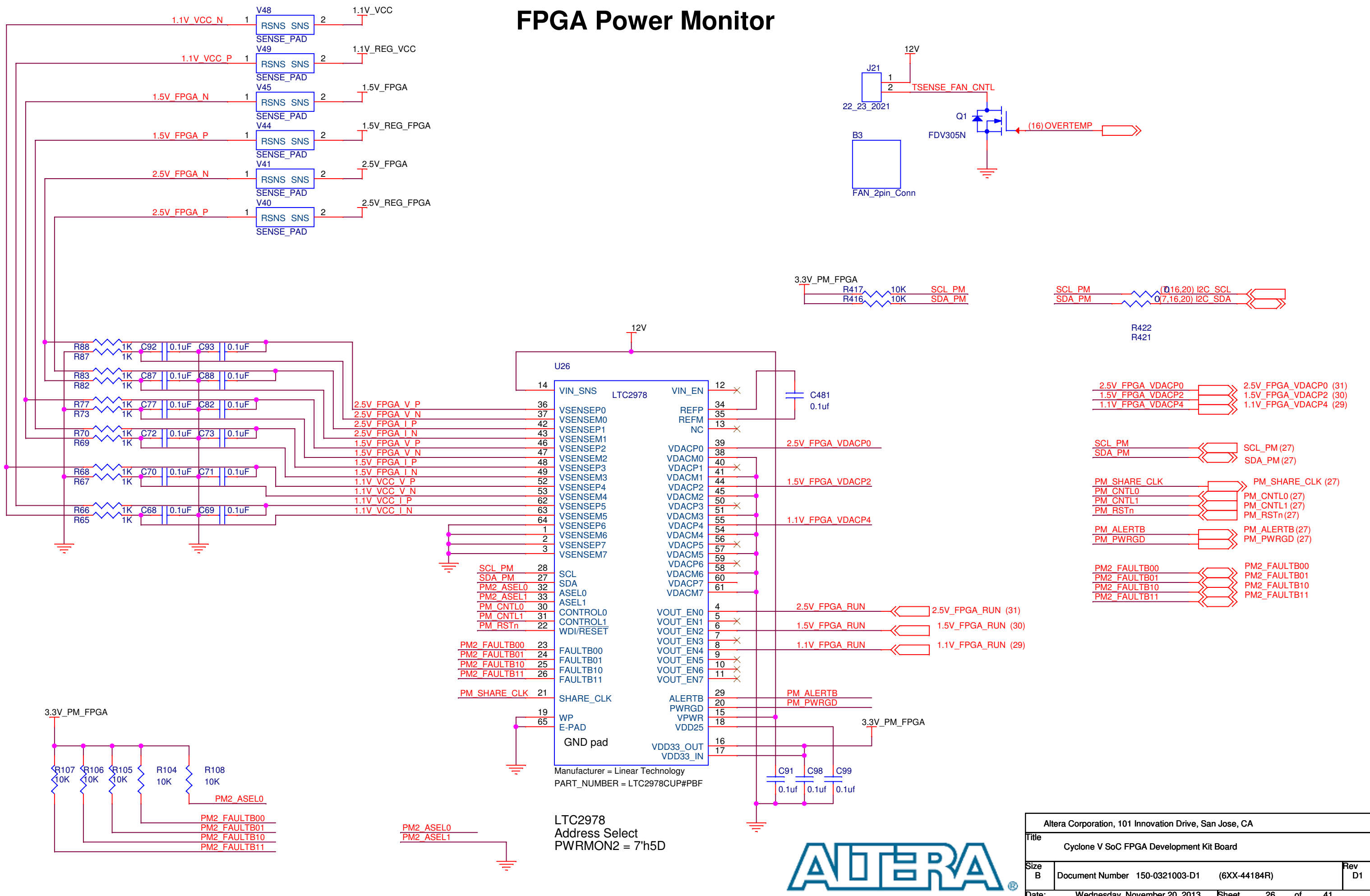
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FPGA Power Monitor

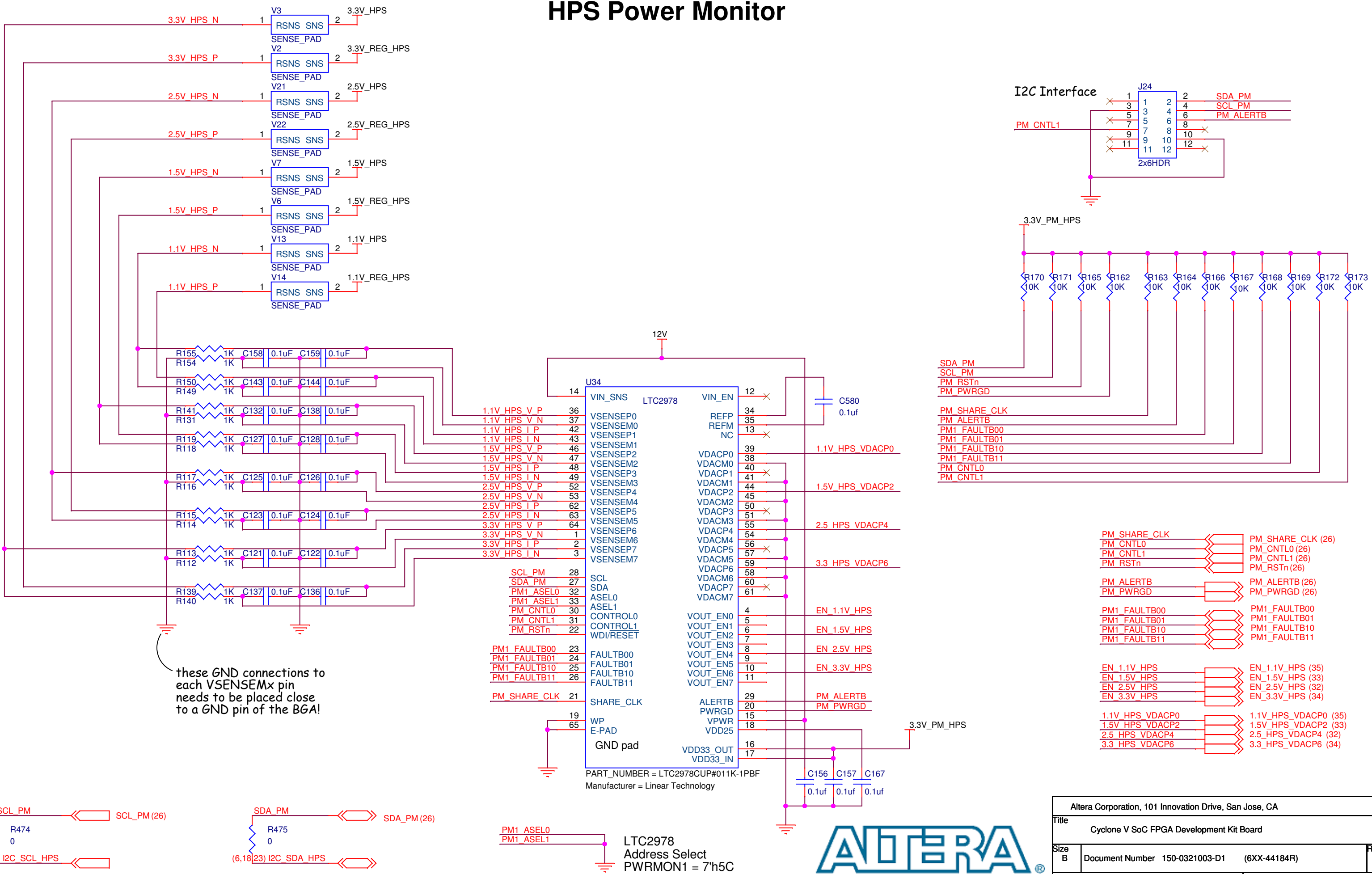


LTC2978
Address Select
PWRMON2 = 7'h5D



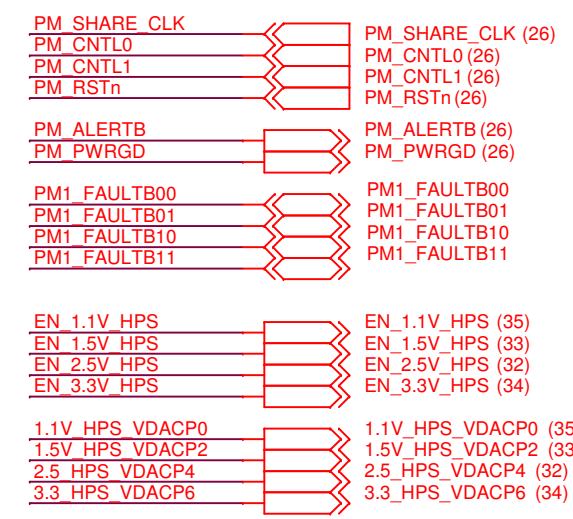
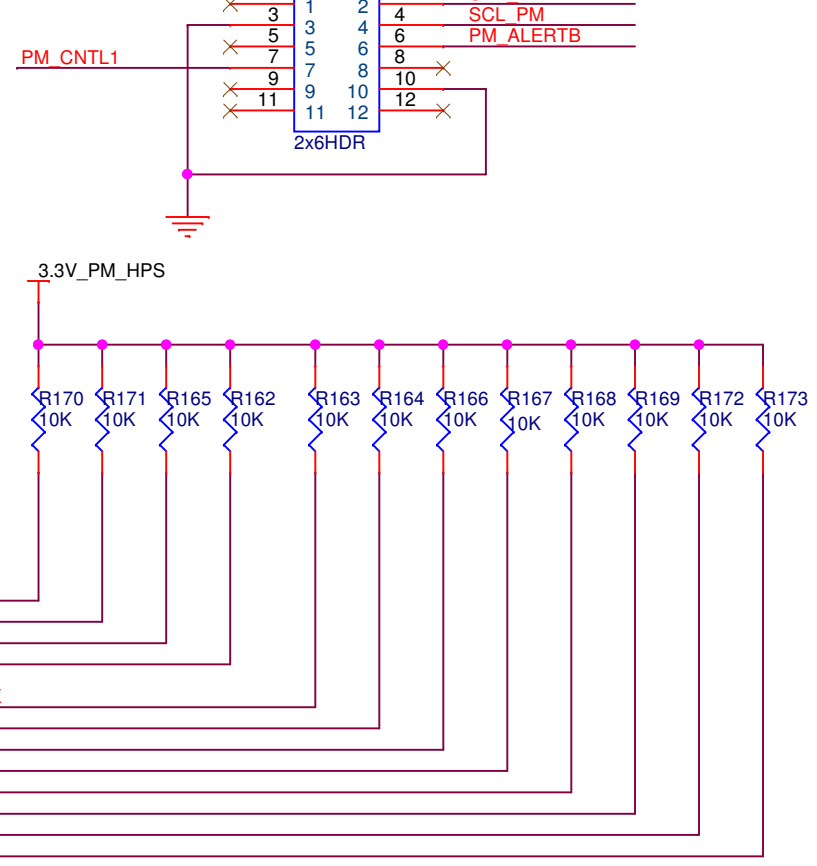
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HPS Power Monitor



these GND connections to each VSENSE_x pin needs to be placed close to a GND pin of the BGA!

I2C Interface



PM1_FAULTB00	23	FAULTB00
PM1_FAULTB01	24	FAULTB01
PM1_FAULTB10	25	FAULTB10
PM1_FAULTB11	26	FAULTB11

PM_SHARE_CLK	21	SHARE_CLK
WP	19	WP
E-PAD	65	E-PAD
GND pad		GND pad

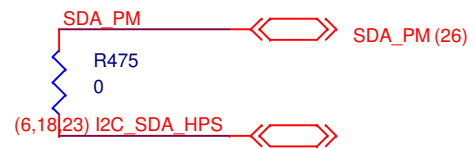
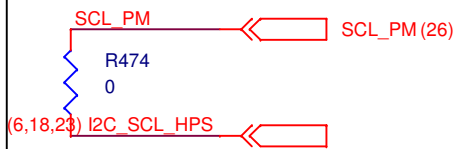
SCL_PM	28	SCL
SDA_PM	27	SDA
PM1_ASEL0	32	ASEL0
PM1_ASEL1	33	ASEL1
PM_CNTL0	30	CONTROL0
PM_CNTL1	31	CONTROL1
PM_RSTn	22	WDI/RESET

PART_NUMBER = LTC2978CUP#011K-1PBF
Manufacturer = Linear Technology

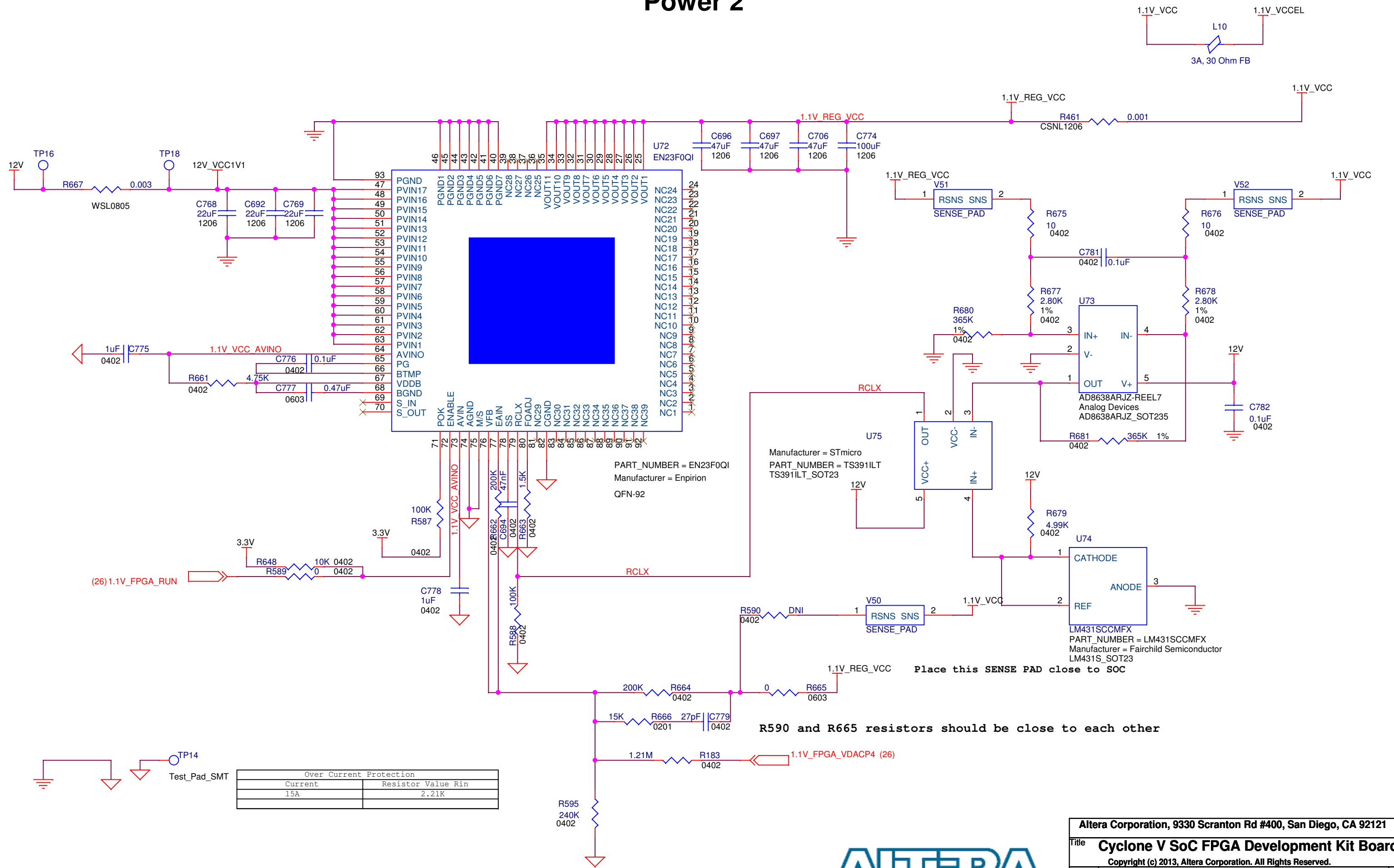
LTC2978
Address Select
PWRMON1 = 7'h5C



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Power 2



PART_NUMBER = EN23F0Q1
 Manufacturer = Enpirion
 QFN-92

Manufacturer = STmicro
 PART_NUMBER = TS391ILT
 TS391ILT_SOT23

Manufacturer = Analog Devices
 AD8638ARJZ-REEL7
 AD8638ARJZ_SOT235

Manufacturer = Fairchild Semiconductor
 PART_NUMBER = LM431SCCMFX
 LM431S_SOT23

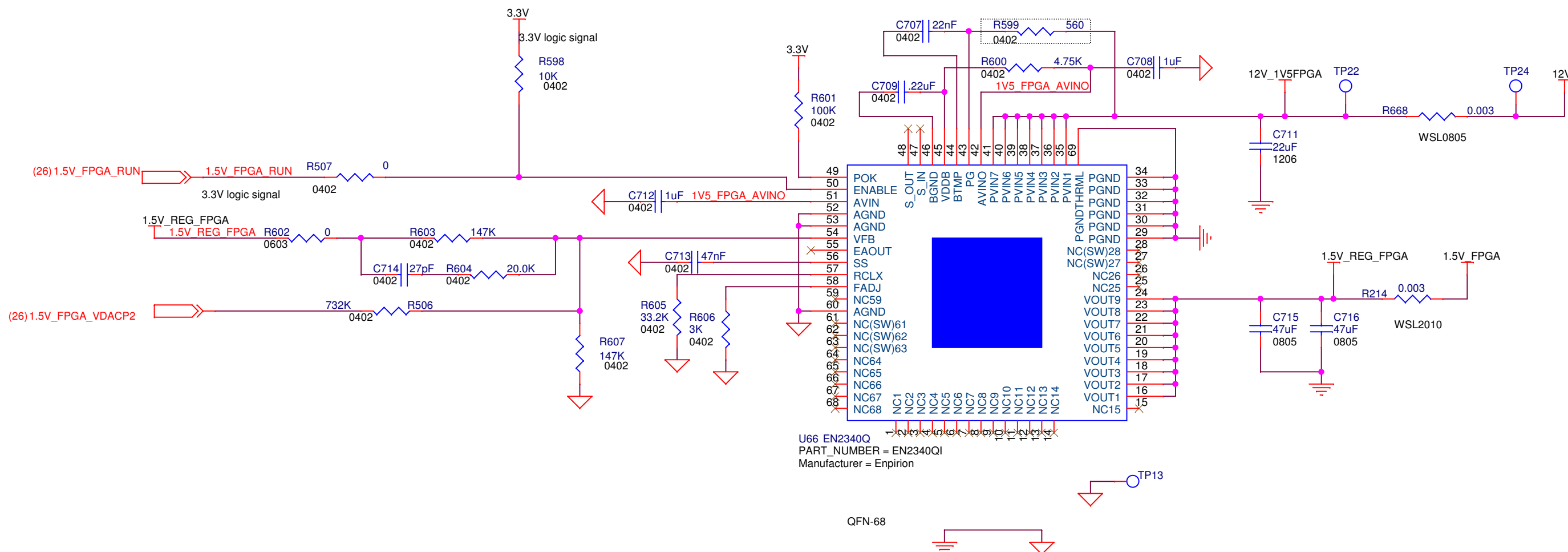
Place this SENSE PAD close to SOC

R590 and R665 resistors should be close to each other

Over Current Protection	
Current	Resistor Value Rin
15A	2.21K

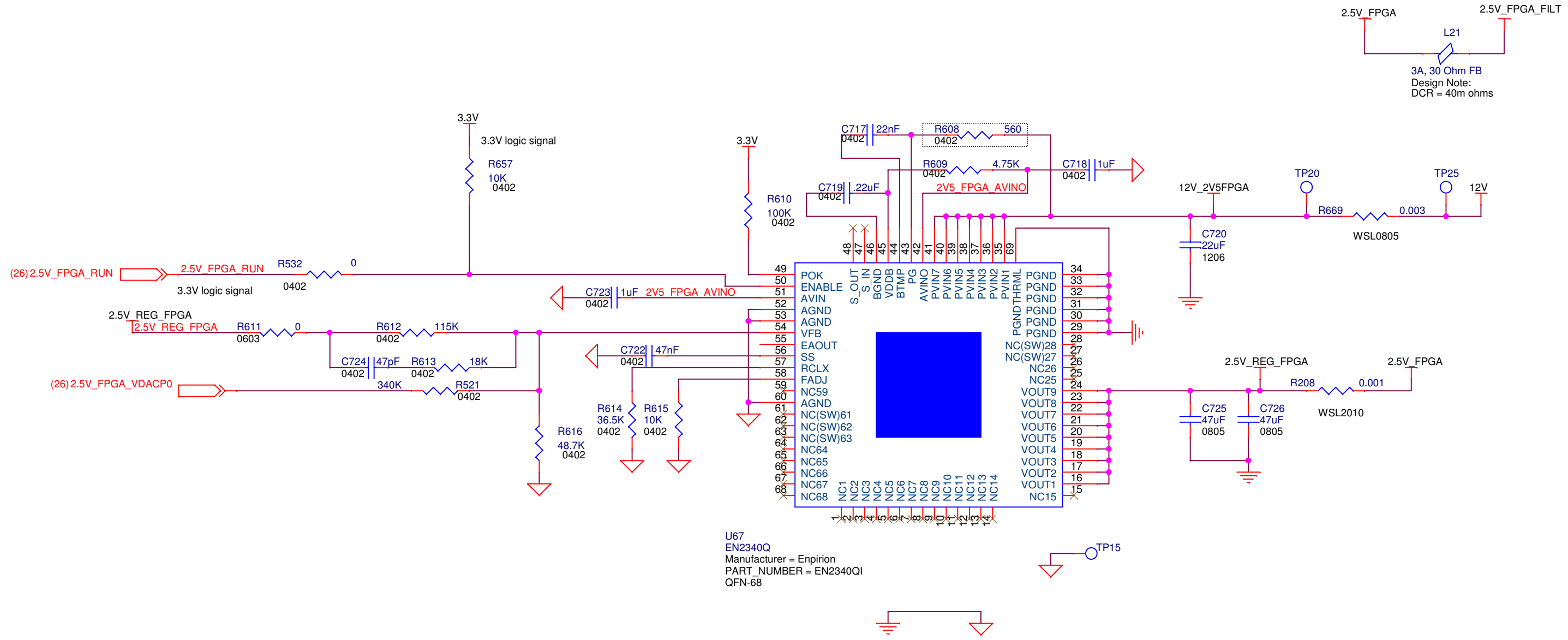


Power 3 - 1.5V FPGA



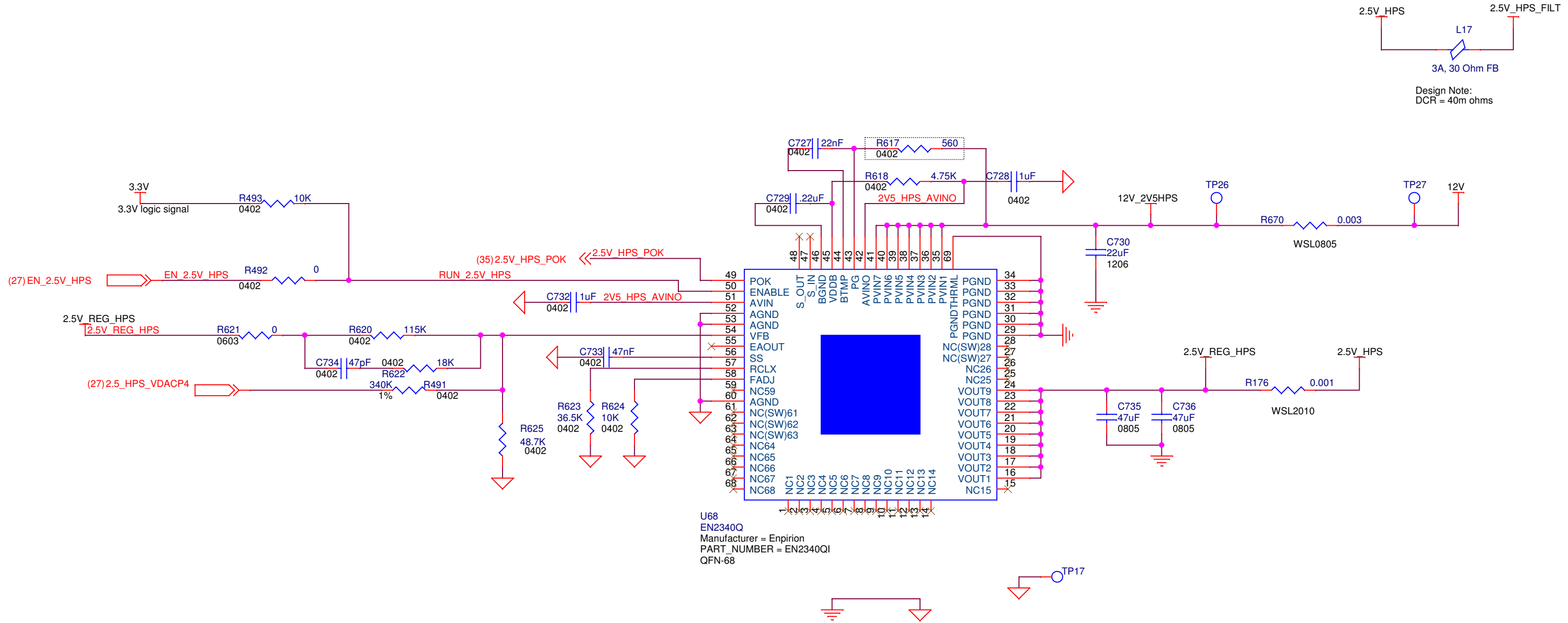
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Power 3 - 2.5V FPGA



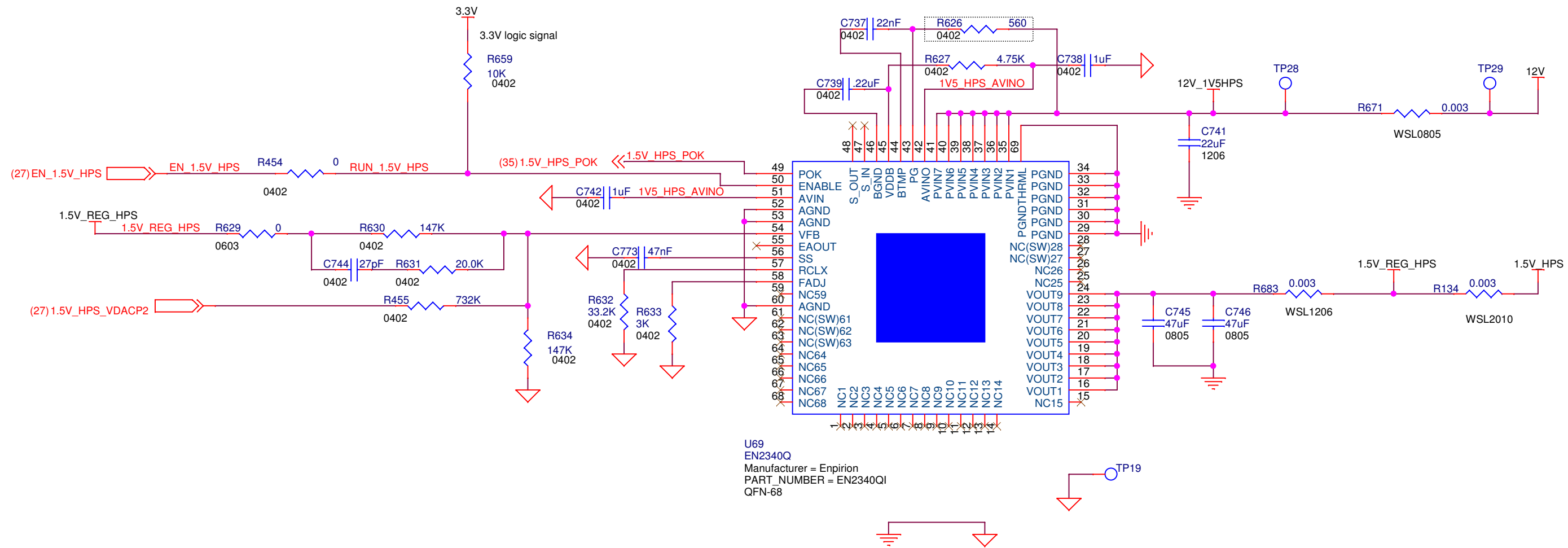
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Power 3 - 2.5V HPS



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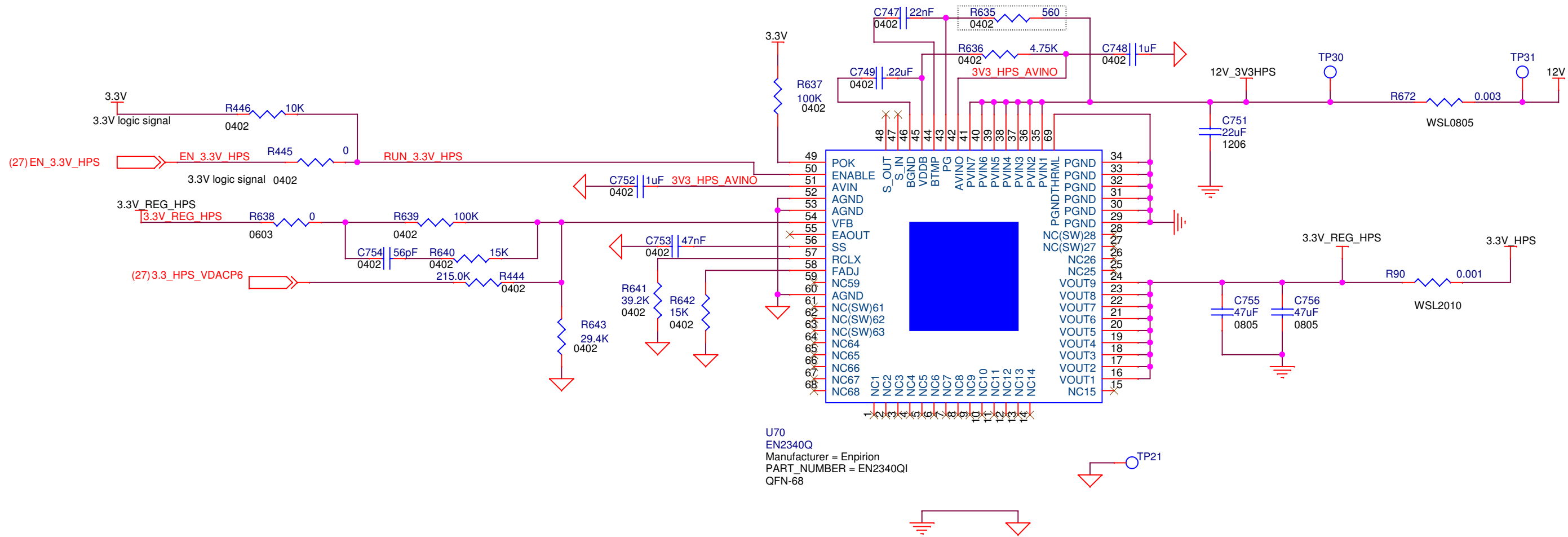
Power 3 - 1.5V & 1.5V HPS



U69
EN2340Q
Manufacturer = Enpirion
PART_NUMBER = EN2340QI
QFN-68

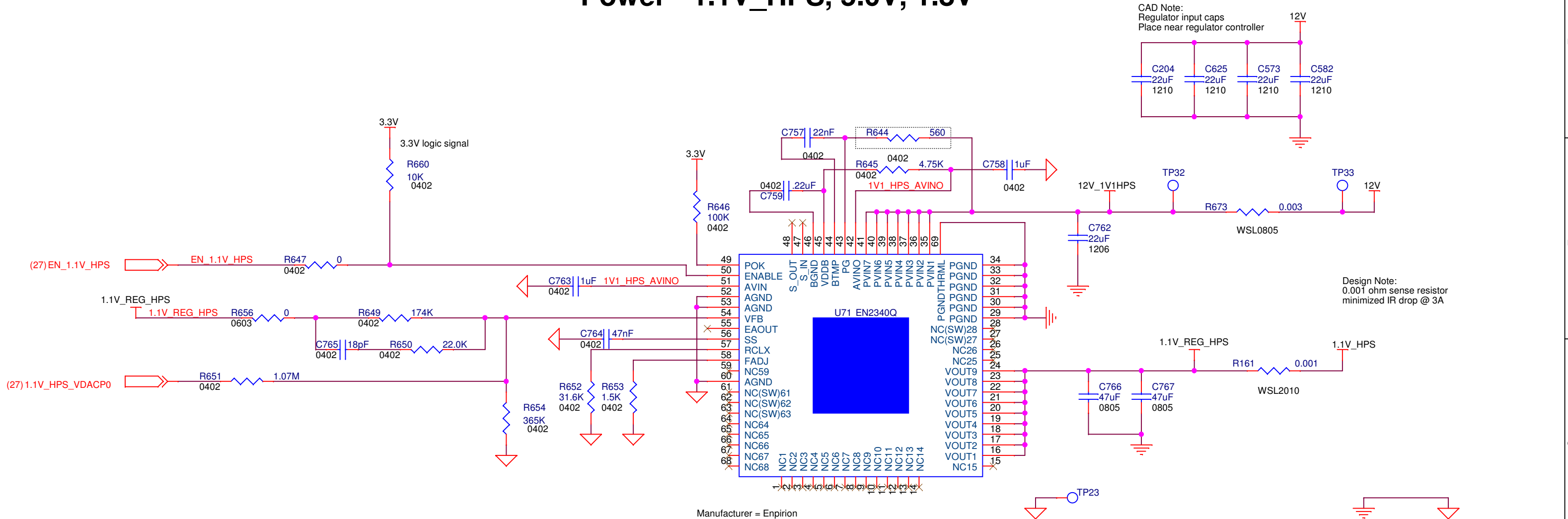


Power 3 - 3.3V HPS

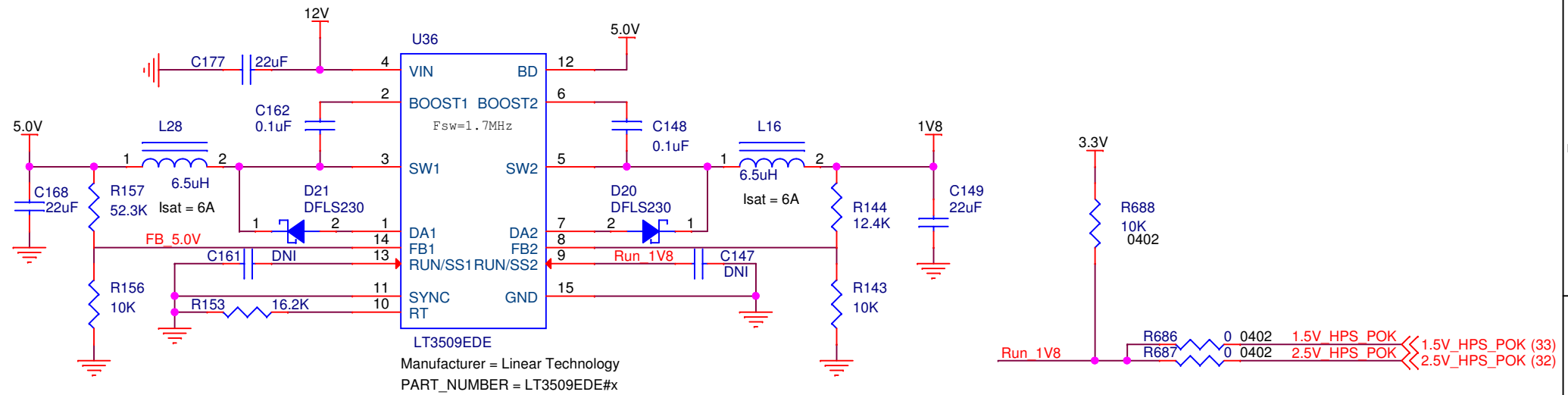


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Power - 1.1V_HPS, 5.0V, 1.8V



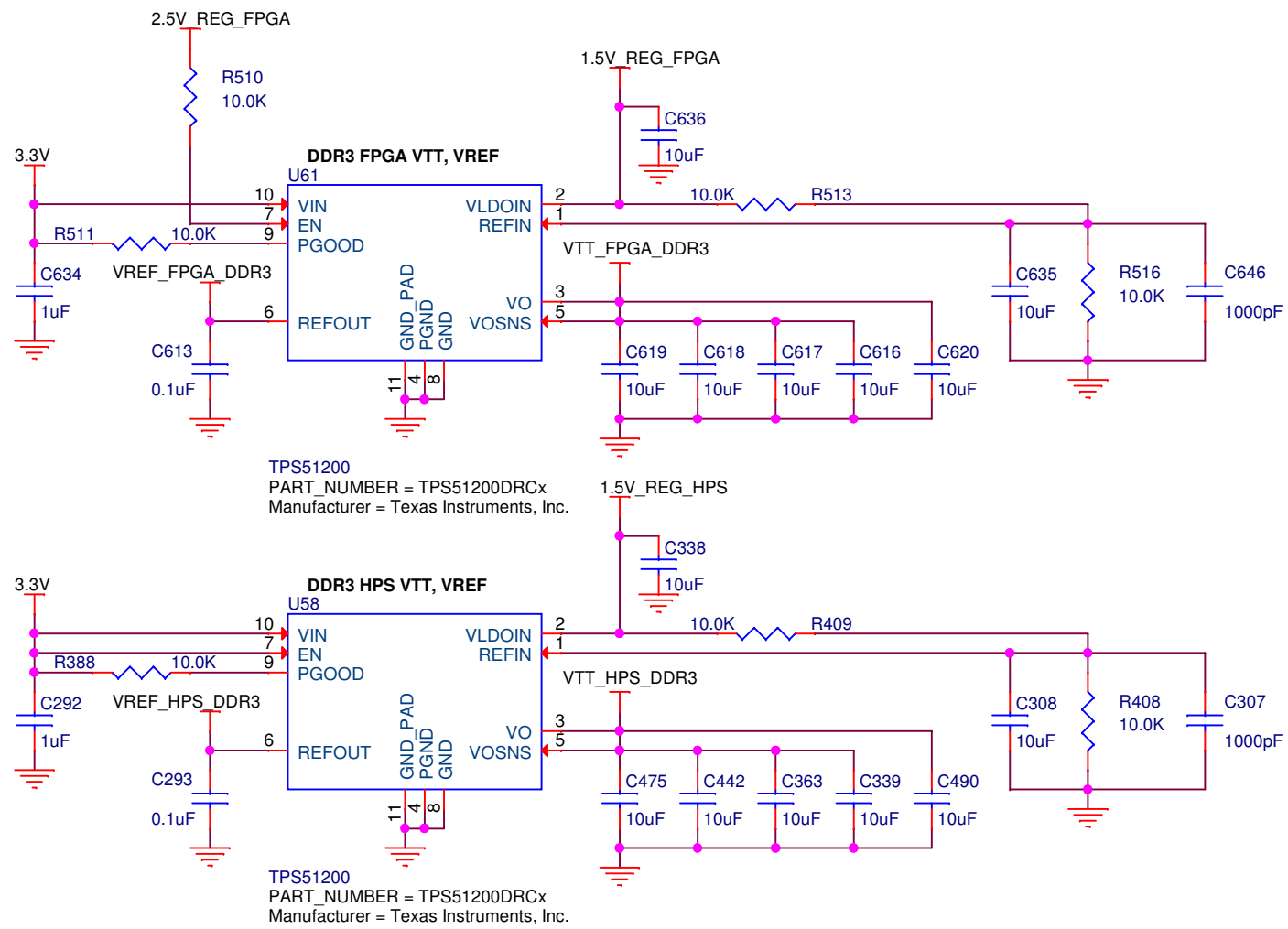
Manufacturer = Enpirion
PART_NUMBER = EN2340QI
QFN-68



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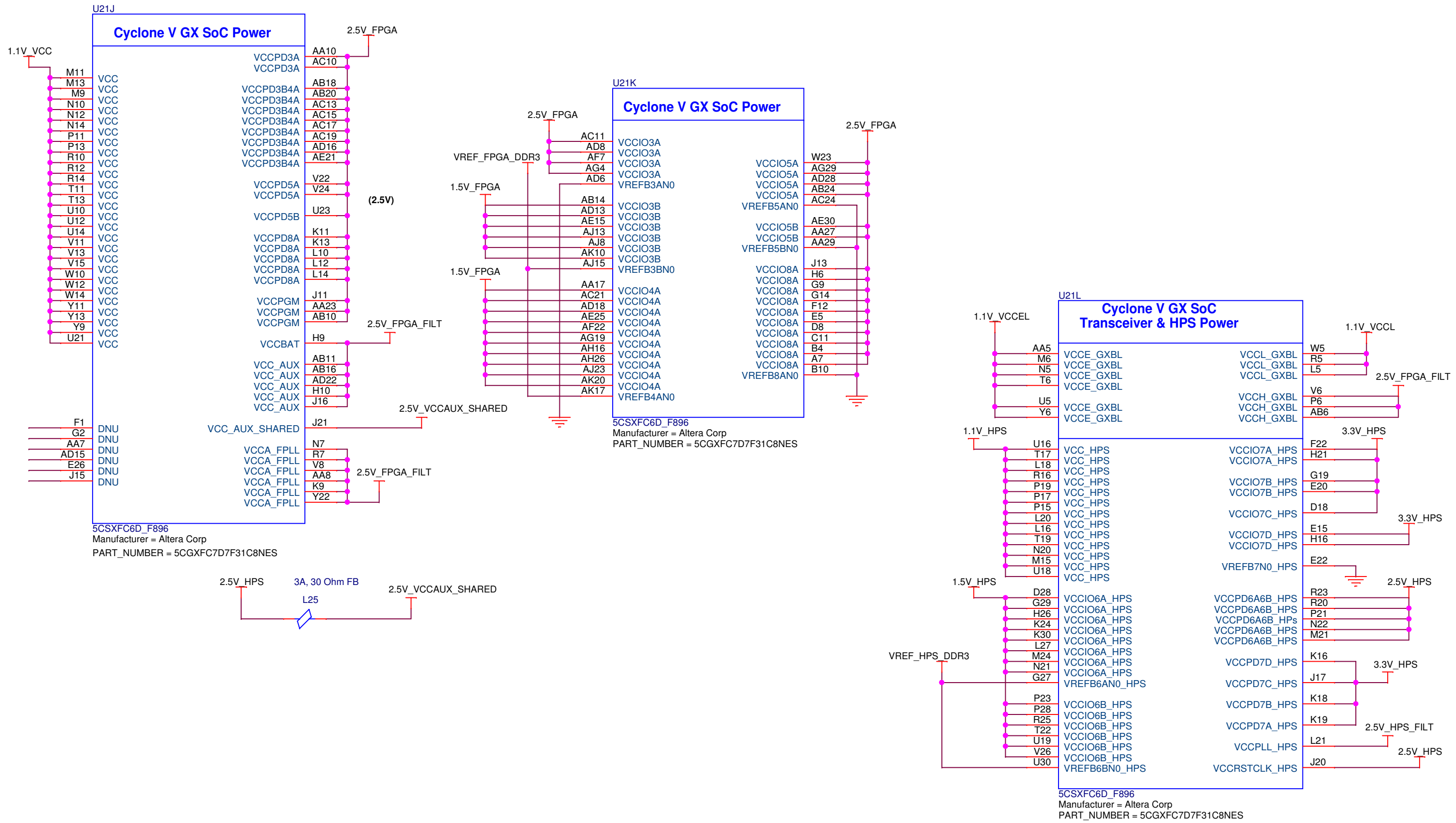
Power 4 - Linear Regulators



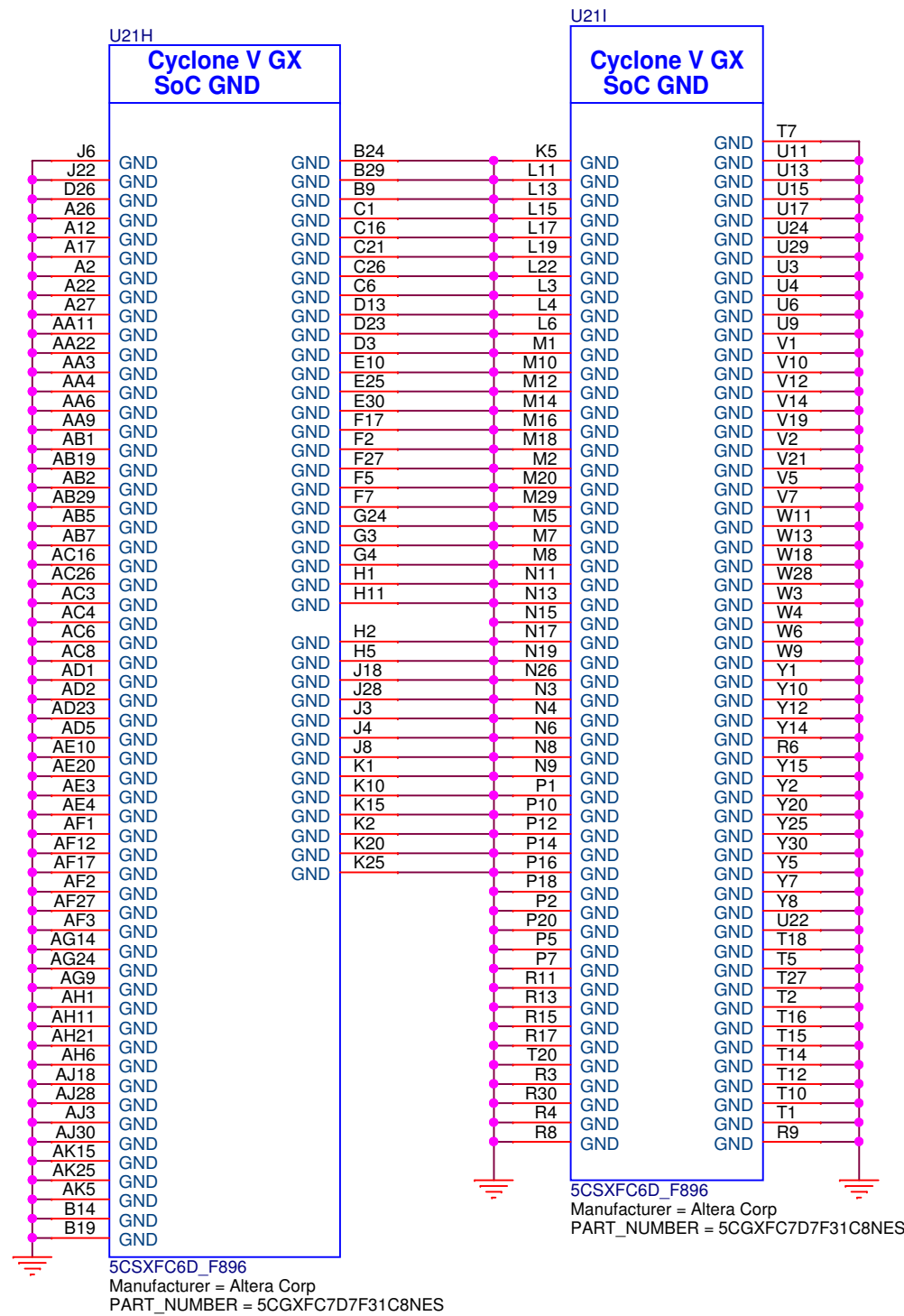
Power 6 - Power & Temperature Monitor

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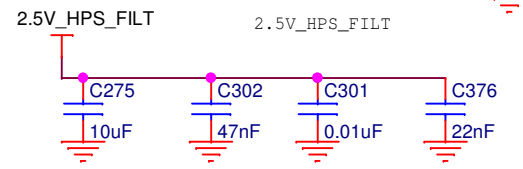
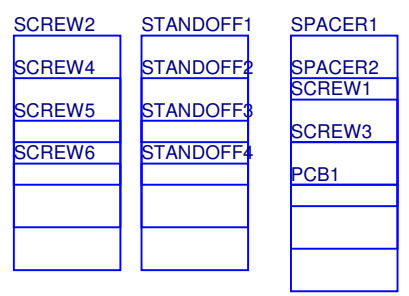
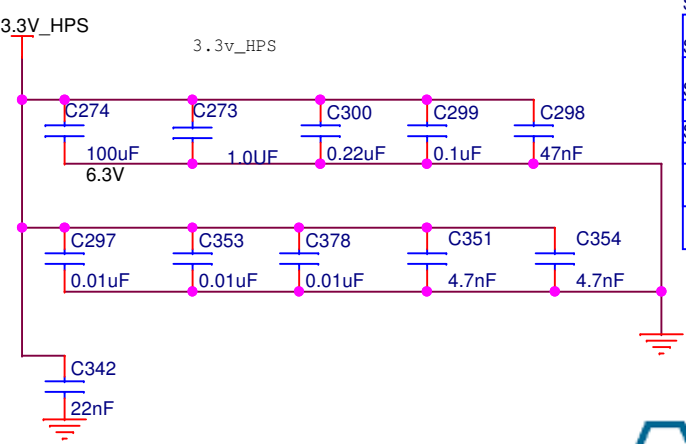
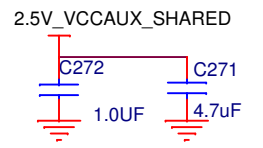
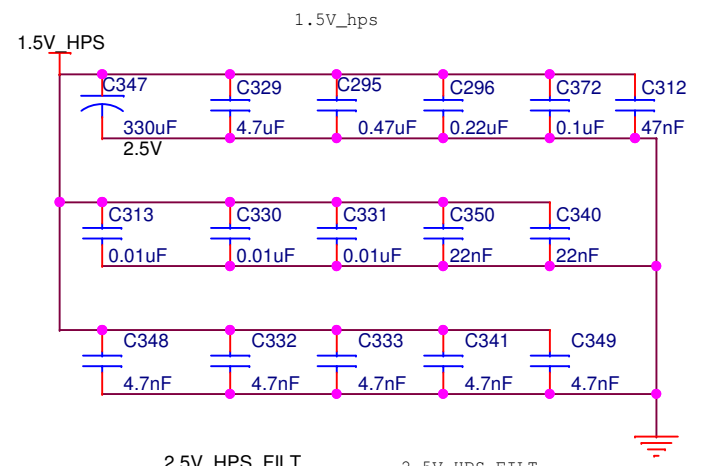
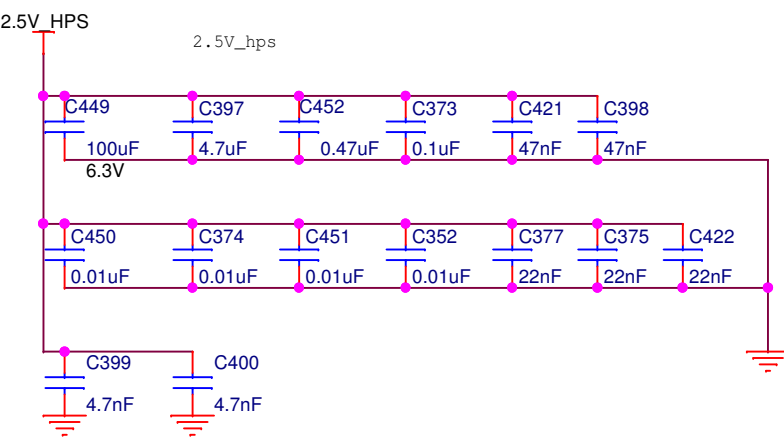
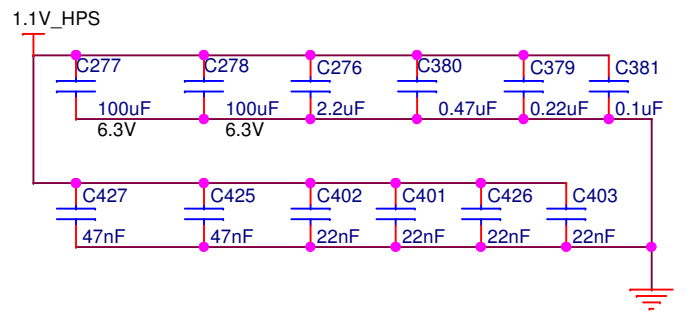
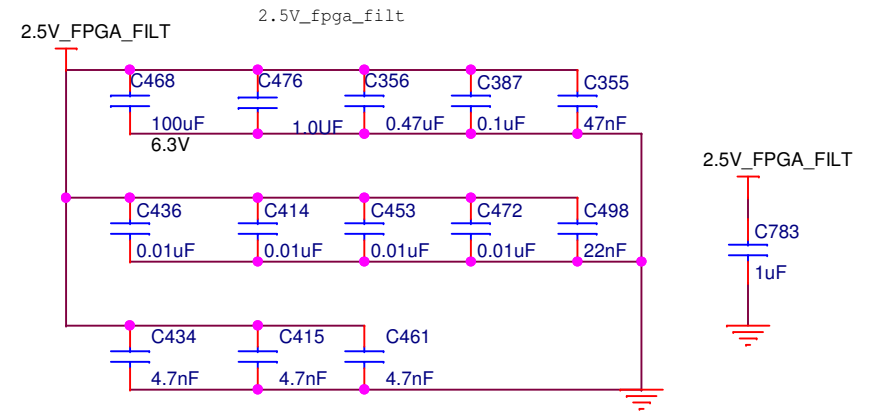
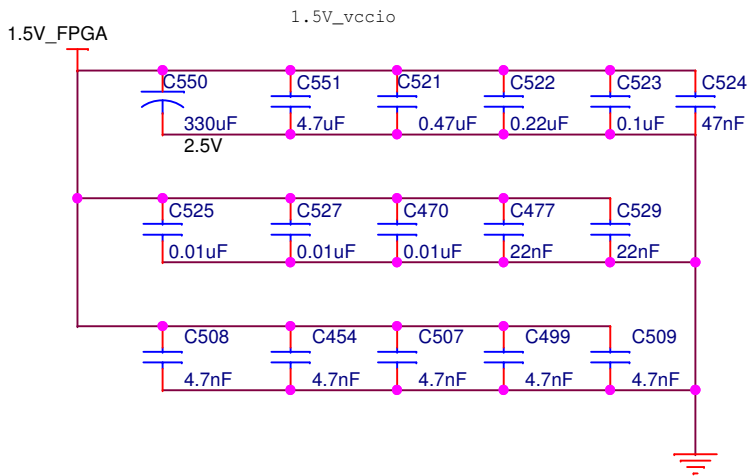
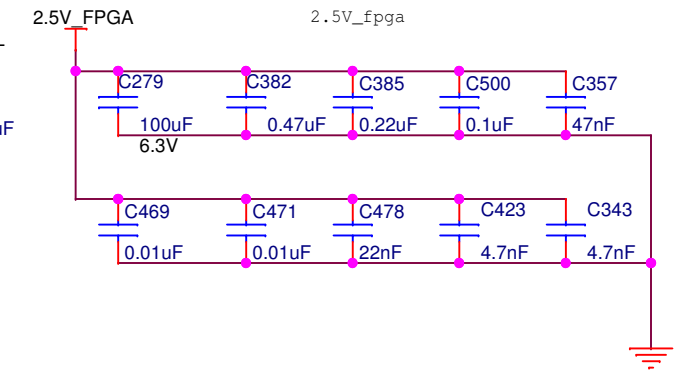
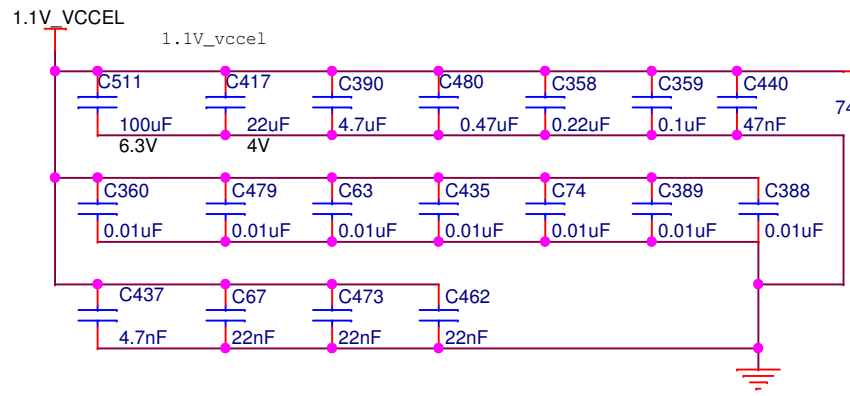
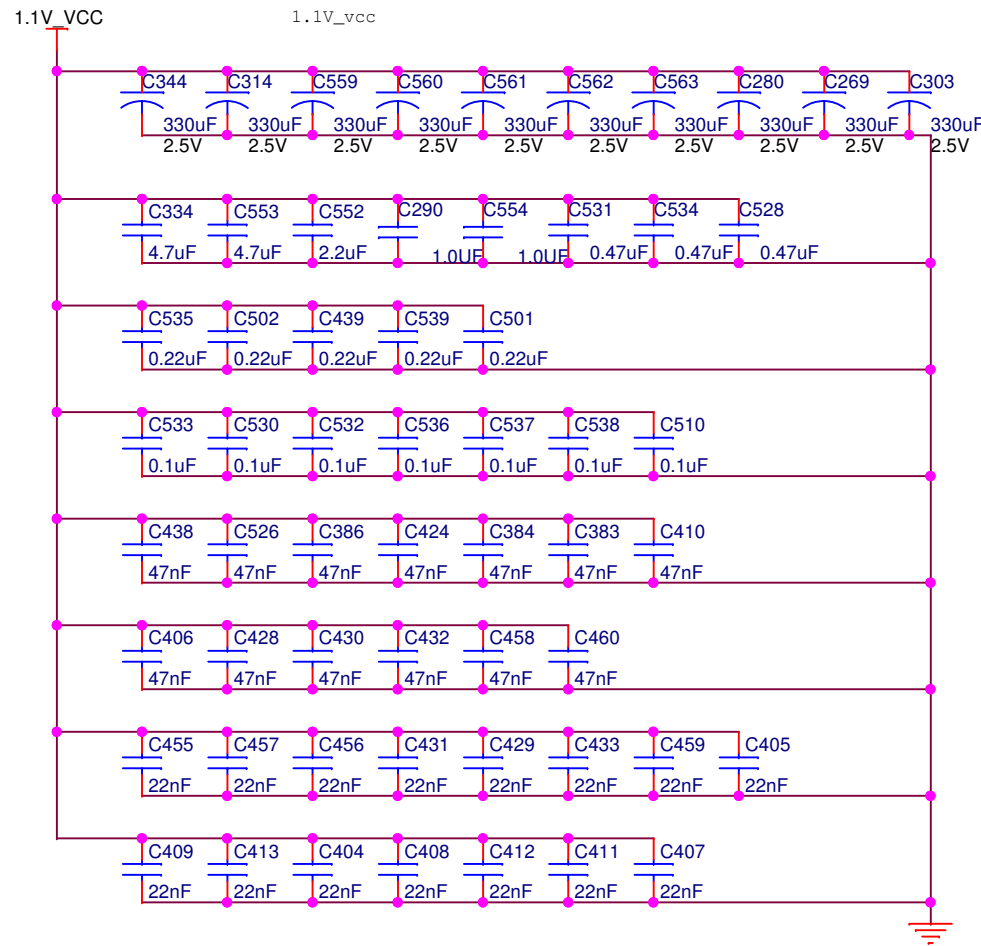
Power 7 - Cyclone V GX SoC Power



Power 8 - Cyclone V GX SoC Ground



Decoupling



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REV	DATE	PAGES	DESCRIPTION
D1	06/28/2013	29-35	Initial version with Enpirion Power Supply
	07/01/2013	30-35	Input cap configuration is changed from 2 x 1206 caps to 1 x 1206 cap
	07/01/2013	30-35	Output cap configuration is changed from 2 x 1206 caps to 2 x 0805 caps
	07/01/2013	29-35	Input sense resistor 1206 size is added
	07/01/2013	29	0 ohm resistor DNL is added for current sensing option at load,OCP circuit is added
	07/03/2013	29-35	Added SMT testpoints at 0 ohm resistor at input rails
	07/03/2013	6	U21.F16 is connected to CODEC_SEL, R32 marked DNL
	07/03/2013	14	R390 and R391 changed to 1K
	07/03/2013	19	R479,R512,R515 changed to 4.7K 1% with load option. R480, R512,R276,R274 marked as DNL.
	07/03/2013	19	R522 is added with 4.7K DNL on RNET2_TX_CLK_FB net. R526,RR525 is changed to 0 Ohm load.
	07/03/2013	21	U5 is changed to N25Q512A83GSF40F. R319 is marked as DNL, R311 is changed to 4.7K
	07/03/2013	22	U1 is cahnged to MAX14523B. Changed C1 to 1uF,C8 to 1uF. C9,C243,C242,C2,C3 were removed.
	07/03/2013	22	J1 change to Micro AB USB type connector.
	07/03/2013	27	Netnames were corrected as per correct power rail name.
	07/10/2013	21	Warm_Reset signal is connected to U5 pin3.
	07/10/2013	6	J32 pin 10 is conncted to 3.3V from 5V
	07/10/2013	35	PIN 9 of U36 pulled to 2.5V HPS.
	07/16/2013	21,16	Connected QSPI reset signal on pin 3 of U5 to pin C11 of the MAX V system controller U19
	07/23/2013	19	R522,R274,R276 is changed to Load from DNL.U45 changed to UPD60620AGK-GAK-AX#YB1
	07/26/2013	30-35	560 Ohm resistors from PG to PVIN on the EN2340 parts are made Install
	07/26/2013	30-35	All the input sense resistors are changed to 0805 size.
	07/26/2013	14,21	R389,R390 changed to 33 ohms. Added 2K pull up on QSPI_RESET signal.
	07/26/2013	22	Added 10K pull up in SD_DAT0.
	07/26/2013	23	R425 is changed to DNI and R434 is changed to 0 ohm load.
	07/26/2013	38	VCC_AUX pins connected to 2.5V_FPGA_FILT from 2.5V_HPS_FILT
	07/26/2013	40	1uF 0402 cap is added on 2.5V_FPGA_FILT net
	08/01/2013	40	Added 10K pullup on SD_DAT0,SD_DAT1,SD_DAT2,SD_CMD. 316K pull down on SD_DAT3.
	08/06/2013	6,17	Added RC termination on JTAG_MUX_TCK and JTAG_HPS_TCK
	08/07/2013	12	Removed DNI resistors from JTAG chain - R343R344,R345,R346,R351,R352,R353,R354,R355,R356,R357,R358,R359,R360,R361,R380,R381,R382,R383,R384,R385,R386,R387,R398,R399,R400,R401,R402,R403,R404,R405.



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